Notes: 1. For each problem, 20% of points is for the “correct” final answer.
2. Messy, incoherent papers lose point! Explain what you are doing!
3. Use the following information only in designing circuits: OpAmps have a unity-gain bandwidth of $10^7$ Hz, a maximum output current limit of 100 mA, and a slew rate of $1 \text{ V/µs}$.
OpAmps are powered by $\pm 15 \text{ V}$ power supplies (power supplies not shown), NPN Si transistors have $\beta = 200$, $\beta_{min} = 100$, $r_\pi = 3 \text{ kΩ}$, and $r_o = 100 \text{ kΩ}$. NMOS transistors have $K = 0.25 \text{ mA/V}^2$ and $V_t = 2 \text{ V}$.
In circuit design, use 5% tolerance commercial resistor and capacitor values of 1, 1.1, 1.2, 1.3, 1.5, 1.6, 1.8, 2, 2.2, 2.4, 2.7, 3, 3.3, 3.6, 3.9, 4.3, 4.7, 5.1, 5.6, 6.2, 6.8, 7.5, 8.2, 9.1 ($\times 10^n$ where $n$ is an integer). You can also use 5 mH inductors.

Problem 1. A) Show that the circuit below is a current source (assume OpAmp is ideal for this part only), B) For $v_s = 2 \text{ V}$ and $R = 10 \text{ kΩ}$, find the maximum $R_L$ that the current source can drive. (10pt)

Part A: Because OpAmp is ideal, $I_p \approx 0$ and $I_n \approx 0$. Then, by KCL, current $i_L$ flows through resistor $R$.
Negative feedback: $v_n \approx v_p = v_s$
Ohm’s law across $R$: $i_L = (v_n - 0)/R = v_s/R = \text{constant}$
Since the output current is a constant and independent of $v_L$ (or $R_L$), this is a current source.
Part B: For $v_s = 2 \text{ V}$ and $R = 10 \text{ kΩ}$, $i_L = 0.2 \text{ mA}$.
Since a DC voltage $v_S$ is applied to the circuit, we only need to consider saturation and maximum current limits:
Maximum output current: $i_L = 0.2 < i_{sc} = 100 \text{ mA}$, does not apply.
Saturation: $v_o \leq v_{sat} = 15$.

$$v_o = (R_L + R)i_L \leq 15$$
$$R_L \leq \frac{15}{i_L} - R = 75 - 10 = 65 \text{ kΩ}$$

Therefore, the maximum $R_L$ that the current source can drive is 65 kΩ.
**Problem 2.** In the circuit below with Si diodes, find \( i \). (10 pt)

![Circuit Diagram]

Note: \( v_1 = v_{D1} \) and \( v_2 = -v_{D2} \) and by KCL

\[
i_1 = i + i_{D1}
\]

\[
i_2 = i + i_{D2}
\]

**Case 1:** Assume both diodes are off \((i_{D1} = i_{D2} = 0, \ v_{D1} < v_\gamma, \text{ and } v_{D2} < v_\gamma)\). We can replace both diodes with open circuit to arrive at the circuit on the right. Then:

\[
i_1 = i \quad \text{and} \quad i_2 = i \quad \text{and} \quad i = \frac{15 - (-15)}{10^3 + 10^3 + 10^3} = 10 \text{ mA}
\]

\[
15 - v_1 = 10^3i = 10 \quad \rightarrow \quad v_{D1} = v_1 = 5 > v_\gamma
\]

Therefore our assumption is incorrect.

**Case 2:** Assume D1 ON and D2 OFF \((v_{D1} = v_\gamma = 0.7 \text{ V}, \ i_{D1} > 0, \ i_{D2} = 0, \text{ and } v_{D2} < v_\gamma)\). We can replace D1 with a voltage source and D2 with an open circuit to arrive at the circuit on the right. Then, noting \( v_1 = v_{D1} = 0.7 \text{ V} \)

\[
i = \frac{v_1 - (-15)}{10^3 + 10^3} = 7.85 \text{ mA}
\]

\[
v_2 - (-15) = 10^3i = 7.85 \quad \rightarrow \quad v_{D2} = -v_2 = +7.15 > v_\gamma
\]

So, assumption of D2 OFF is NOT justified.

**Case 3:** Assume D1 OFF and D2 ON \((v_{D1} < v_\gamma, \ i_{D1} = 0, \ v_{D2} = v_\gamma = 0.7 \text{ V}, \text{ and } i_{D2} > 0)\). (see circuit). Then, noting \( v_2 = -v_{D1} = -0.7 \text{ V} \)

\[
i = i_1 = \frac{15 - v_2}{10^3} = 15.7 \text{ mA}
\]

\[
15 - v_1 = 10^3i = 7.85 \quad \rightarrow \quad v_{D1} = v_1 = +7.15 > v_\gamma
\]
So, assumption of D1 OFF is NOT justified.

**Case 4:** Assume D1 and D2 are both ON ($v_{D1} = v_{D2} = v_\gamma = 0.7$ V, $i_{D1} > 0$, and $i_{D2} > 0$). Then, noting $v_1 = v_{D1} = 0.7$ V and $v_2 = -v_{D1} = -0.7$ V

$$i_1 = \frac{15 - v_1}{10^3} = 14.3 \text{ mA}$$

$$i_2 = \frac{v_2 - (-15)}{10^3} = 14.3 \text{ mA}$$

$$i = \frac{v_1 - (-v_2)}{10^3} = 1.4 \text{ mA}$$

$$i_{D1} = i_1 - i = 12.9 \text{ mA} > 0$$ and $$i_{D2} = i_2 - i = 12.9 \text{ mA} > 0$$

Therefore our assumptions are justified and D1 and D2 are ON and $i = 1.4$ mA.

**Problem 3.** In the circuit below, $V_{tn} = \bar{V}_t$, $V_{tp} = -\bar{V}_t$, both transistors have the same $K$ value, and $V_{DD} > 2\bar{V}_t$. Prove that this circuit is a NOT gate. (10pt)

1) by KVL $v_{GS1} = v_i$ and $v_{GS2} = v_i - v_{DD}$,
2) by KVL $v_o = v_{DS1} = V_{DD} - v_{DS2}$.
3) by KCL $i_{D1} = i_{D2}$.

$v_i = 0$ Since $v_{GS1} = v_i = 0 < \bar{V}_t$, NMOS will be in cut-off and $i_{D1} = 0$. On the other hand, $v_{GS2} = v_i - V_{DD} = -V_{DD} < -\bar{V}_t$ and PMOS will be ON. But $i_{D2} = i_{D1} = 0$. Since PMOS is ON and $i_{D2} = 0$, PMOS should in Ohmic state and $v_{DS2} = 0$. Output voltage can now be found by KVL: $v_o = V_{DD} - v_{DS2} = V_{DD}$. So, when $v_i = 0$, $v_o = V_{DD}$.

$v_i = V_{DD}$ Since $v_{GS1} = v_i = V_{DD} > \bar{V}_t$, NMOS will be ON. On other hand, $v_{GS2} = v_i - V_{DD} = 0 > -\bar{V}_t$, PMOS will be in cut-off, and $i_{D2} = 0$. Since $i_{D1} = i_{D2} = 0$ and NMOS is ON, NMOS should be in ohmic state with $v_{DS1} = 0$. Then $v_o = v_{DS1} = 0$. So, when $v_i = V_{DD}$, $v_o = 0$.

Therefore, this is a NOT gate as when $v_i = 0$, $v_o = V_{DD}$ and when $v_i = V_{DD}$, $v_o = 0$. 

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**Problem 4.** Design a filter with the transfer function of \( H(j\omega) = \frac{-3}{1 - j50,000/\omega} \) and input impedance \( \geq 20 \text{k}\Omega \). (10 pts)

The transfer function is in the general form for first-order high-pass filters:

\[
H(j\omega) = \frac{K}{1 - j\omega_c/\omega}
\]

with \( K = -3 \) and \( \omega_c = 50,000 \text{ rad/s} \). As \( |K| > 1 \), we need to use an active filter. The prototype of the circuit is shown below with

\[
H(j\omega) = -\frac{R_2/R_1}{1 - j\omega_c/\omega} \quad \omega_c = R_1C_1
\]

The input impedance of this filter is \( Z_{i|\text{min}} = R_1 \).

Comparing the transfer function of this prototype circuit with the desired one, we get:

\[
\frac{R_2}{R_1} = 3
\]

\[
\omega_c = \frac{1}{R_1C_1} = 50,000
\]

\[
Z_{i|\text{min}} = R_1 \geq 20 \text{k}\Omega
\]

Choosing commercial value of \( R_1 = 20 \text{k}\Omega \), we get:

\[
R_2 = 3R_1 = 60 \text{k}\Omega \rightarrow 62\text{k}\Omega \quad \text{(Commercial)}
\]

\[
C_1 = \frac{1}{50,000R_1} = \frac{1}{5 \times 10^4 \times 2 \times 10^4} = 1.0 \times 10^{-9} \rightarrow 1 \text{nF} \quad \text{(Commercial)}
\]

We need to consider the impact of the bandwidth of OpAmp chip. \( A \times f_c = f_u = 10^7 \) leads to \( f_c = 10^7/(1 + 3) = 2500 \gg f_u = 50/(2\pi) = 8 \text{ kHz} \). So the circuit should work properly.
Problem 5. (A) Find the Q-point parameters of both transistors in the circuit shown (assume $K = 200 \, \mu A/V^2$ and $V_t = 2 \, V$). (12 pt)

Part A: Replacing the biasing resistors of Q1 and $R_2$ with its Thevenin equivalent, we get:

$$R_G = R_1 \parallel R_2 = \frac{20 \times 10^3 \times 82 \times 10^3}{20 \times 10^3 + 82 \times 10^3} = 16.0 \, \text{k}\Omega$$

$$V_{GG} = \frac{20 \times 10^3}{20 \times 10^3 + 82 \times 10^3} \times 20 = 3.9 \, \text{V}$$

Since $I_{G1} = I_{G2} = 0$, current $I_{D1}$ flows in the 1 k source resistor of Q1. Then,

$$\text{GS1-KVL} \quad V_{GG} = R_G I_{G1} + V_{GS1} + 10^3 I_{D1} \quad \rightarrow \quad V_{GS1} + 10^3 I_{D1} = 3.9$$

Assuming that Q1 is in active, we have $I_{D1} = K(V_{GS1} - V_t)^2 = 200 \times 10^{-6}(V_{GS1} - 2)^2$. Substituting for $I_{D1}$ in GS1-KVL, we get:

$$V_{GS1} + 10^3 \times 200 \times 10^{-6}(V_{GS1} - 2)^2 = 3.9$$

$$5V_{GS1} + (V_{GS1} - 2)^2 = 19.6$$

$$V_{GS1}^2 + V_{GS1} - 15.6 = 0$$

which give two roots of $-4.48$ and $3.48 \, \text{V}$. The negative root is not correct ($< V_t$). Thus, $V_{GS1} = 3.48$ and $I_{D1} = 200 \times 10^{-6}(V_{GS1} - 2)^2 = 0.44 \, \text{mA}$ and

$$\text{DS1-KVL} \quad V_{DD} = V_{DS1} + 10^3 I_{D1} \quad \rightarrow \quad V_{DS1} = 20 - 0.44 = 19.56 \, \text{V}$$

Since $V_{DS1} = 19.56. > V_{GS1} - V_t = 3.48 - 2 = 1.48 \, \text{V}$, our assumption of Q1 active is correct.

$$\text{GS2-KVL} \quad V_{DD} = V_{DS1} + V_{GS2} + 500 I_{D2} \quad \rightarrow \quad V_{GS2} + 500 I_{D2} = 20 - 19.56 = 0.44$$

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Since the sum of $V_{GS2} + 500I_{D2}$ is quite small, Q2 is probably in cut-off (check first). Assuming that Q2 is in cut-off, $I_{D2} = 0$ and $V_{GS2} < V_t$. Substituting for $I_{D2} = 0$ in GS2-KVL above, we find $V_{GS2} = 0.44 < V_t = 2$ V. Therefore, our assumption of Q2 in cut-off is correct. Then,

$$\text{DS2-KVL } V_{DD} = 2 \times 10^3 I_{D2} + V_{DS2} + 500I_{D2} \rightarrow V_{DS2} = 20 \text{ V}$$

Thus, Q1 is in active state with $I_{D1} = 0.8 \text{ mA}$, $V_{GS1} = 8.0 \text{ V}$, and $V_{DS1} = 12. \text{ V}$ and Q2 is in cut-off with $I_{D2} = 0$, $V_{GS2} = 0.44 \text{ V}$, and $V_{DS2} = 20 \text{ V}$.

**Problem 6.** Consider the circuit below with a Si BJT, and $v_Z > v_\gamma$. A) Show that this circuit is a current source (i.e., $i_L$ is independent of $R_L$) as long as the diode is in the Zener region. (You can assume that when BJT is ON, $i_E \approx i_c$). (6pt)

KVL through BE terminals and Zener diode gives:

$$R_iE - v_{BE} + v_D = 0$$

For diode is in Zener region, $v_D = -v_Z$ and $i_D < 0$. Assuming that the PNP transistor is ON: $v_{BE} = -v_\gamma$:

$$i_E = \frac{v_Z - v_\gamma}{R} = const$$

Since $i_E > 0$, assumption of BJT ON is justified. Then, $i_L = i_c \approx i_E = const$ and is independent of $R_L$. Therefore, this circuit is a current source as long as the diode stays in the Zener region.
Problem 7. Design a BJT amplifier with a gain of 3 and a cut-off frequency of 50 Hz. Set the operating point (Q-point) parameters to be $V_{CE} = 8$ V and $I_c = 4$ mA. (12pt)

The prototype of this circuit is a common emitter amplifier with an emitter resistance.

DC bias: To set the Q-point in the middle of load line, set $V_{CC} = 2V_{CE} = 16$ V.

$$V_{CC} = R_CI_C + V_{CE} + R_EI_E$$

$$16 - 8 = 4 \times 10^{-3}(R_C + R_E) \quad \rightarrow \quad R_C + R_E = 2.0 \text{ k} \Omega$$

$$A_v = \frac{R_C}{R_E} = 3$$

$$4R_E + R_E = 2.0 \text{ k} \Omega \quad \rightarrow \quad R_E = 500 \text{ } \Omega, \ R_C = 1.5 \text{ k} \Omega$$

Commercial values are $R_E = 510 \Omega$ and $R_C = 1.5 \text{ k} \Omega$.

Check for good biasing $V_E > 1$ V: $V_E = R_EI_E = 510 \times 4 \times 10^{-3} = 2 > 1$, it is OK.

$R_B$ and $V_{BB}$:

$$R_B \ll (\beta + 1)R_E \quad \rightarrow \quad R_B = 0.1(\beta_{min} + 1)R_E = 0.1 \times 101 \times 510 = 5.1 \text{ k} \Omega$$

KVL:

$$V_{BB} = R_BI_B + V_{BE} + R_EI_E$$

$$V_{BB} = 5.1 \times 10^3\frac{4 \times 10^{-3}}{201} + 0.7 + 510 \times 4 \times 10^{-3} = 2.84 \text{ V}$$

$R_1$ and $R_2$:

$$R_B = R_1 || R_2 = \frac{R_1R_2}{R_1 + R_2} = 5.1 \text{ k} \Omega$$

$$\frac{V_{BB}}{V_{CC}} = \frac{R_2}{R_1 + R_2} = \frac{2.84}{16} = 0.18$$

$R_1 = 28.7 \text{ k} \Omega$ and $R_2 = 6.2 \text{ k} \Omega$. Commercial values are $R_1 = 30 \text{ k} \Omega$ and $R_2 = 6.2 \text{ k} \Omega$.

Design values are: $R_1 = 30 \text{ k} \Omega, \ R_2 = 6.2 \text{ k} \Omega, \ R_E = 510 \text{ } \Omega, \text{ and } R_C = 1.5 \text{ k} \Omega$. As the lower cut-off frequency is not specified, we cannot specify any value for $C_c$.

$$R_i \approx R_B = 5.1 \text{ k} \Omega$$

$$\omega_l = 2\pi50 = \frac{1}{R_iC_c} \quad \rightarrow \quad C_c = 6.2 \times 10^{-7} = 620 \text{ n} \F$$

Design values are: $R_1 = 33 \text{ k} \Omega, \ R_2 = 6.2 \text{ k} \Omega, \ R_E = 510 \text{ } \Omega, \ R_C = 2.4 \text{ k} \Omega, \text{ and } C_c = 680\text{nF}$. 

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