Problem 1. The circuit below has a Si transistor with $\beta = 200$ and $V_A = 100$ V.
A) Find $R_E$ such that $I_C = 2$ mA. B) Find the circuit gain, $R_i$, $R_o$, and $f_l$.

This is a common-collector amplifier (input at the base, output at the emitter) which is biased with two power supplies.

A) Bias): we set $v_{sig} = 0$, and open the capacitor.

$$I_C \approx I_E = 2 \text{ mA } \quad I_B = I_C/\beta = 10 \text{ } \mu\text{A}$$

EB-KVL: $0 = 10^3 I_B + V_{BE} + R_E I_E - 3$

$$0 = 10^3 \times 10 \times 10^{-6} + 0.7 + 2 \times 10^{-3} R_E - 3$$

$$R_E = 1.15 \text{ k}$$

EC-KVL: $3 = V_{CE} + R_E I_E - 3 \rightarrow V_{CE} = 3.70 \text{ V} > V_D0 \text{ (active)}$

B) Amp parameters: First, we calculate the small-signal parameters:

$$g_m = \frac{I_C}{V_T} = \frac{2 \times 10^{-3}}{26 \times 10^{-3}} = 76.9 \text{ mA/V},$$

$$r_o = \frac{V_A}{I_C} = \frac{100}{2 \times 10^{-3}} = 50.0 \text{ k} \quad r_\pi = \frac{\beta}{g_m} = 2.60 \text{ k}$$

In a common-collector amplifier or emitter follower (Note $R_B = \infty$):

$$\frac{v_o}{v_i} = \frac{g_m(r_o \parallel R_E \parallel R_L)}{1 + g_m(r_o \parallel R_E \parallel R_L)}$$

$$r_o \parallel R_E \parallel R_L = 50.0 \text{ k} \parallel 1.15 \text{ k} \parallel 20 \text{ k} = 1.06 \text{ k}$$

$$g_m(r_o \parallel R_E \parallel R_L) = 81.5 \quad \frac{v_o}{v_i} = \frac{81.5}{1 + 81.5} = 0.988$$

$$R_i = R_B \| [r_\pi + \beta(r_o \parallel R_E \parallel R_L)] = 2.60 \text{ k} + 200 \times 1.06 \text{ k} = 215 \text{ k}$$

$$R_o = R_E \| r_o \| \frac{r_\pi + R_E}{1 + \beta} = 1.15 \text{ k} \| 50.0 \text{ k} \| 18.0 = 17.7 \Omega$$

$$\frac{v_o}{v_{sig}} = \frac{R_i}{R_i + R_{sig}} \times \frac{v_o}{v_i} = \frac{215 \text{ k}}{215 \text{ k} + 1 \text{ k}} \times 0.988 = 0.983$$

$$f_l = f_{p2} = \frac{1}{2\pi(R_L + R_o)C_{c2}} = \frac{1}{2\pi(20 \times 10^3 + 17.7)100 \times 10^{-9}} = 79.5 \text{ Hz}$$
Problem 2. Find $v_o$ in terms of $v_i$ in the circuit below with Si diodes.

Method 1: If we switch the position of D2 and 1-k resistor (as is shown), it is clear that the combination of D1 and 1-k resistor is a rectifier circuit. Diode D2 acts as a clipper which wants to remove voltage below $-0.7$ V (D2 is ON when clipping occurs). As the output of the rectifier part does not include any negative voltages, the clipper diode is never turned ON and is always OFF (i.e., open circuit). As such the original circuit reduces to the rectifier part only and

For: $v_i < 0.7$ V  
$v_o = 0$  
D1 & D2 are both OFF

For: $v_i \geq 0.7$ V  
$v_o = v_i - 0.7$ V  
D1 is ON and D2 is OFF

Method 2: As D1 is the only connection between $v_i$ and D2/resistor combination, we consider its states first:

D1 OFF: $v_{D1} < 0.7$ V, $i_{D1} = 0$. In this case, D2 and the 1k resistor are disconnected from any voltage/current sources and, thus, have zero currents and voltages. Therefore, $v_o = 0$. Also, D2 will be off as $v_{D2} = -v_o = 0$.

$v_{D1} = v_i - v_o = v_i \rightarrow v_{D1} < 0.7 \rightarrow v_i < 0.7$ V

D1 ON: $v_{D1} = 0.7$ V, $i_{D1} \geq 0$. By KCL, $i_1 = i_{D1} + i_{D2}$. Since $i_D$ cannot be negative, $i_1 \geq 0$. Thus, $v_o = 10^3 i_1 \geq 0$ and $v_{D2} = -v_o \leq 0$. Therefore, D2 will be OFF ($i_{D2} = 0$, $i_1 = i_{D1}$) and

$v_o = v_i - 0.7$ V

$\Omega$-law: 
\[
i_{D1} = i_1 = \frac{v_o}{10^3} = \frac{v_i - 0.7}{10^3}
\]

$i_{D1} \geq 0 \rightarrow v_i \geq 0.7$ V

Thus:

For: $v_i < 0.7$ V  
$v_o = 0$  
D1 & D2 are both OFF

For: $v_i \geq 0.7$ V  
$v_o = v_i - 0.7$ V  
D1 is ON and D2 is OFF
Problem 3. Find $v_o$ for $v_i = 0$ V ($V_{tp} = -2$ V, $\mu_pC_{ox}(W/L) = 0.5$ mA/V², and $\lambda = 0$).

\[ v_{SG} = 12 - 0 = 12 \text{ V} \]
\[ V_{OV} = v_{SG} - |V_{tp}| = 12 - 2 = 10 \text{ V} \]

Since $V_{OV} > 0$, assume PMOS in saturation:

\[ i_D = 0.5\mu_pC_{ox}(W/L)V_{OV}^2 = 0.5 \times 0.5 \times 10^{-3} \times (10)^2 = 25 \text{ mA} \]

DS-KVL:
\[ 12 = v_{SD} + 2 \times 10^3i_D \implies v_{SD} = -38 \text{ V} \]

Since $v_{SD} = -38 < V_{OV}$, PMOS is NOT in saturation. Assume PMOS in triode:

\[ i_D = 0.5\mu_pC_{ox}(W/L)(2v_{SD}V_{OV} - v_{SD}^2) \]

DS-KVL:
\[ 12 = v_{SD} + 2 \times 10^3i_D = v_{SD} + 20 \times 10^{-3} \times 0.5 \times 0.5 \times 10^{-3} \times (20v_{SD} - v_{SD}^2) \]
\[ \implies 0.5v_{SD}^2 - 11v_{SD} + 12 = 0 \implies v_{SD} = 20.8 \text{ V \ and \ } v_{SD} = 1.15 \text{ V} \]

$v_{SD} = 20.8$ V is unphysical ($v_{SD} \geq V_{OV} = 10$ V). Thus, $v_o = 12 - v_{SD} = 10.85$ V.

Problem 4. Consider the circuit below with a Si transistor with $\beta = 100$ and $V_A = \infty$ and a Si Zener diode with $V_Z = 5$V. Find $V_{CE}$.

We assume that the diode is in Zener region: $v_D = -V_Z = -5$ V and $i_D \leq 0$. We also assume that transistor is in active. Since $V_B = -v_D = 5$ V:

BE-KVL:
\[ V_B = 5 = V_{BE} + 10^3I_E \]
\[ I_E = 4.3 \text{ mA} \implies I_C \approx I_E = 4.3 \text{ mA} \]

CE-KVL:
\[ 15 = 10^3I_C + V_{CE} + 10^3I_E \implies V_{CE} = 15 - 8.6 = 6.4 \text{ V} \]

Since $V_{CE} = 6.4 > V_{D0} = 0.7$ V, assumption of BJT in active is justified.

To show that the diode is in Zener region:

KCL:
\[ I_B = I_1 + i_D \implies i_D = I_B - I_1 \]

Ω-law:
\[ I_1 = \frac{15 - V_B}{10 \times 10^3} = \frac{15 - 5}{10^4} = 1 \text{ mA} \]
\[ I_B = I_C/\beta = 4.3 \times 10^{-3}/100 = 43 \mu\text{A} \]
\[ i_D = I_B - I_1 = 43 \times 10^{-6} - 10^{-3} = -0.957 \text{ mA} \]

Since $i_D < 0$, assumption of diode in Zener region is also justified.

Solution of ECE65 Final B (Winter 2013)
Problem 5. Find the circuit gain, $R_i$, $R_o$, and $f_L$ ($V_{tp} = -1$ V, $\mu_p C_{ox}(W/L) = 8$ mA/V$^2$, $\lambda = 0.01$ V$^{-1}$ and ignore channel width modulation in biasing).

This is a common-gate amplifier (input at the source, output at the drain) which is biased with two power supplies.

**Bias:** we set $v_{sig} = 0$, and open the capacitor.

$$I_D = 0.5\mu_p C_{ox}(W/L)V_{OV}^2 = 4 \times 10^{-3}V_{OV}^2$$

SG-KVL: $6 = 10^3 I_D + v_{SG} + 0$

$6 = 10^3 \times 4 \times 10^{-3}V_{OV}^2 + V_{OV} + |V_{tp}|$

$4V_{OV} + V_{OV} - 5 = 0 \rightarrow V_{OV} = 1.0$ V

$I_D = 4 \times 10^{-3}V_{OV}^2 = 4$ mA  

SD-KVL: $6 = 10^3 I_D + V_{SD} + 10^3 I_D - 6 \rightarrow V_{SD} = 4$ V $> V_{OV} = 1$ saturation

$$g_m = \frac{2I_D}{V_{OV}} = 8.00 \text{ mA/V} \quad r_o = \frac{1}{\lambda I_D} = 25 \text{ k}$$

In a common-gate amplifier (Note $R_G = \infty$):

$$\frac{v_o}{v_i} = g_m(r_o \parallel R_D \parallel R_L)$$

$r_o \parallel R_D \parallel R_L = 25 \text{ k} \parallel 1 \text{ k} \parallel 10 \text{ k} = 877 \Omega \quad \rightarrow \quad \frac{v_o}{v_i} = 8.00 \times 10^{-3} \times 877 = 7.02$

$$R_i = R_S \parallel \frac{1 + (R_D \parallel R_L)/r_o}{g_m}$$

$$\frac{1 + (R_D \parallel R_L)/r_o}{g_m} = \frac{1.04}{8 \times 10^{-3}} = 130 \Omega \quad \rightarrow \quad R_i = 1 \text{ k} \parallel 130 = 115 \Omega$$

$R_o = R_D \parallel [r_o(1 + g_m(R_S \parallel R_{sig}))] \quad \rightarrow \quad R_o = 1 \text{ k} \parallel 43.2 \text{ k} = 977 \Omega$

$$\frac{v_o}{v_{sig}} = \frac{R_i}{R_i + R_{sig}} \times \frac{v_o}{v_i} = \frac{115}{115 + 100} \times 7.02 = 3.75$$

$$f_{p1} = \frac{1}{2\pi(R_i + R_{sig})C_{c1}} = \frac{1}{2\pi(115 + 100) \times 100 \times 10^{-9}} = 7.40 \text{ kHz}$$

$$f_{p2} = \frac{1}{2\pi(R_L + R_o)C_{c2}} = \frac{1}{2\pi(10 \times 10^3 + 977) \times 100 \times 10^{-9}} = 145 \text{ Hz}$$

$f_l = f_{p1} + f_{p2} = 7.55 \text{ kHz}$

Solution of ECE65 Final B (Winter 2013)
**Problem 6.** Find the circuit gain, $R_i$, and $R_o$. Si BJTs with $\beta_1 = 100$, $\beta_2 = 50$, and $V_{A1} = V_{A2} = \infty$.

This is a two-stage amplifier. Both stages are in the common-collector configuration (input at the base, output at the emitter). Both are biased with emitter degeneration. Q1 is biased with a voltage divider and Q2 is directly biased from Q1. Note that BJTs are arranged as a Darlington pair with $i_{E1} = i_{B2}$.

**Bias:** Bias circuit (capacitors open) is shown above right in which Q1 voltage divider bias circuit is replaced with its Thevenin equivalent:

$$R_B = 300 \, k \parallel 450 \, k = 180 \, k$$

$$V_{BB} = \frac{450 \, k}{300 \, k + 450 \, k} \times 15 = 9.00 \, V$$

Assuming that both transistors are in active:

$$I_{E2} \approx I_{C2} = \beta_2 I_{B2} = \beta_2 I_{E1} = \beta_1 \beta_2 I_{B1} = 5,000 I_{B1}$$

**BE-KVL:**

$$V_{BB} = 9 = 180 \times 10^3 I_{B1} + V_{BE1} + V_{BE2} + 470 I_{E2}$$

$$7.6 = (180 \times 10^3 + 470 \times 5,000) I_{B1} \quad \rightarrow \quad I_{B1} = 3.00 \, \mu A$$

$$I_{E1} \approx I_{C1} = \beta_1 I_{B1} = 0.300 \, mA \quad \rightarrow \quad I_{B2} = I_{E1} = 3.00 \, \mu A$$

$$I_{E2} \approx I_{C2} = \beta_2 I_{B2} = 15.0 \, mA$$

We need to justify our assumption of both BJTs in active by computing $V_{CE1}$ and $V_{CE2}$:

**CE1-KVL:**

$$15 = V_{CE1} + V_{BE2} + 470 I_{E2} = V_{CE1} + 0.7 + 7.05$$

$$V_{CE1} = 7.25 \, V \quad \text{ (> 0.7 : Q1 active)}$$

**CE2-KVL:**

$$15 = V_{CE2} + 470 I_{E2} = V_{CE1} + 7.05$$

$$V_{CE2} = 7.95 \, V \quad \text{ (> 0.7 : Q2 active)}$$
\[ g_{m1} = \frac{I_{C1}}{V_T} = 11.5 \text{ mA/V}, \]
\[ r_o1 = \frac{V_{A1}}{I_{C1}} = \infty \]
\[ r_{\pi 1} = \frac{\beta_1}{g_{m1}} = 8.67 \text{ k} \]
\[ g_{m2} = \frac{I_{C2}}{V_T} = \frac{15.0 \times 10^{-3}}{26 \times 10^{-3}} = 577 \text{ mA/V}, \]
\[ r_o2 = \frac{V_{A2}}{I_{C2}} = \infty \quad \text{and} \quad r_{\pi 2} = \frac{\beta_2}{g_{m2}} = 86.7 \text{ } \Omega \]

Signal circuit is shown above. Both stages are emitter follower. To find the circuit gain and \( R_i \), we start from the load side (\( R_{L2} = R_L = 10 \text{ k} \)). Note that \( R_{B2} = \infty \).

\[ \frac{v_{o2}}{v_{i2}} = \frac{g_{m2}(r_o2 \parallel R_{E2} \parallel R_{L2})}{1 + g_{m2}(r_o2 \parallel R_{E2} \parallel R_{L2})} \quad r_o2 \parallel R_{E2} \parallel R_{L2} = 470 \parallel 10 \text{ k} = 449 \text{ } \Omega \]
\[ g_{m2}(r_o2 \parallel R_{E2} \parallel R_{L2}) = 259 \quad \Rightarrow \quad \frac{v_{o2}}{v_{i2}} = \frac{259}{1 + 259} = 0.996 \]
\[ R_{i2} = R_{B2} \parallel [r_{\pi 2} + \beta_2(r_o2 \parallel R_{E2} \parallel R_{L2})] = 86.7 + 50 \times 449 = 22.5 \text{ } \Omega \]

Setting \( R_{L1} = R_{i2} = 22.5 \text{ k} \) and noting \( R_{E1} = \infty \):

\[ \frac{v_{o1}}{v_{i1}} = \frac{g_{m1}(r_o1 \parallel R_{E1} \parallel R_{L1})}{1 + g_{m1}(r_o1 \parallel R_{E1} \parallel R_{L1})} \quad r_o1 \parallel R_{E1} \parallel R_{L1} = R_{L1} = 22.5 \text{ k} \]
\[ g_{m1}(r_o1 \parallel R_{E1} \parallel R_{L1}) = 259 \quad \Rightarrow \quad \frac{v_{o1}}{v_{i1}} = \frac{259}{1 + 259} = 0.996 \]
\[ R_{i1} = R_{B1} \parallel [r_{\pi 1} + \beta_1(r_o1 \parallel R_{E1} \parallel R_{L1})] = 180 \text{ k} \parallel 2.26 \text{ M} = 167 \text{ k} \]

To find \( R_o \), we start from the source side (\( R_{\text{sig}1} = R_{\text{sig}2} = 1 \text{ k} \)).

\[ R_o1 = R_{E1} \parallel r_o1 \parallel \frac{r_{\pi 1} + R_{B1} \parallel R_{\text{sig}1}}{1 + \beta_1} = \frac{(8.67 \text{ k} + 180 \text{ k} \parallel 1 \text{ k})}{101} = 95.7 \text{ } \Omega \]
\[ R_{\text{sig}2} = R_{o1} = 95.7 \text{ } \Omega \]
\[ R_o2 = R_{E2} \parallel r_o2 \parallel \frac{r_{\pi 2} + R_{B2} \parallel R_{\text{sig}2}}{1 + \beta_2} = 470 \parallel (86.7 + 95.7)/51 = 3.55 \text{ } \Omega \]
Parameters of the two-stage amplifier are:

\[
R_i = R_{i1} = 167 \text{ k}
\]
\[
R_o = R_{o2} = 3.55 \Omega
\]
\[
\frac{v_o}{v_{\text{sig}}} = \frac{R_i}{R_i + R_{\text{sig}}} \times \frac{v_{o1}}{v_{i1}} \times \frac{v_{o2}}{v_{i2}} = \frac{167 \text{ k}}{167 \text{ k} + 1 \text{ k}} \times 0.996 \times 0.996 = 0.986
\]