

BJT Amplifier Circuits

As we have developed different models for DC signals (simple large-signal model) and AC signals (small-signal model), analysis of BJT circuits follows these steps:

DC biasing analysis: Assume all capacitors are open circuit. Analyze the transistor circuit using the simple large signal mode as described in pp 57-58.

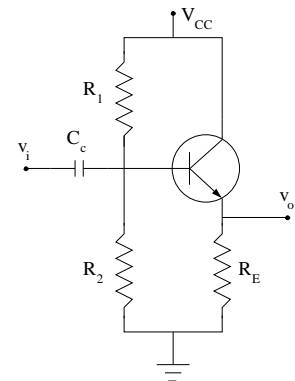
AC analysis:

- 1) Kill all DC sources
- 2) Assume coupling capacitors are short circuit. The effect of these capacitors is to set a lower cut-off frequency for the circuit. This is analyzed in the last step.
- 3) Inspect the circuit. If you identify the circuit as a prototype circuit, you can directly use the formulas for that circuit. Otherwise go to step 3. 3) Replace the BJT with its small signal model.
- 4) Solve for voltage and current transfer functions and input and output impedances (node-voltage method is the best).
- 5) Compute the cut-off frequency of the amplifier circuit.

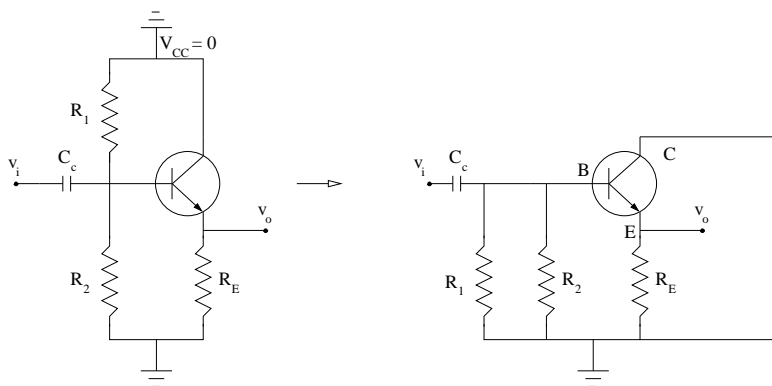
Several standard BJT amplifier configurations are discussed below and are analyzed. Because most manufacturer spec sheets quote BJT “h” parameters, I have used this notation for analysis. Conversion to notation used in most electronic text books (r_{π} , r_o , and g_m) is straight-forward.

Common Collector Amplifier (Emitter Follower)

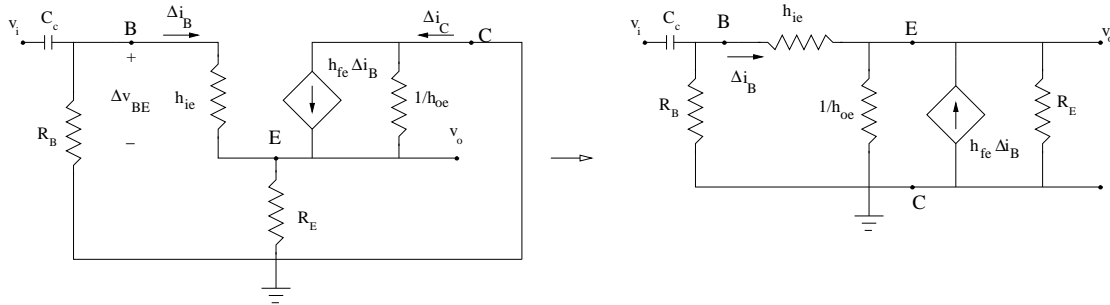
DC analysis: With the capacitors open circuit, this circuit is the same as our good biasing circuit of page 79 with $R_c = 0$. The bias point currents and voltages can be found using procedure of pages 78-81.



AC analysis: To start the analysis, we kill all DC sources:



We can combine R_1 and R_2 into R_B (same resistance that we encountered in the biasing analysis) and replace the BJT with its small signal model:



The figure above shows why this is a common collector configuration: collector is shared between input and output AC signals. We can now proceed with the analysis. Node voltage method is usually the best approach to solve these circuits. For example, the above circuit will have only one node equation for node at point E with a voltage v_o :

$$\frac{v_o - v_i}{r_\pi} + \frac{v_o - 0}{r_o} - \beta \Delta i_B + \frac{v_o - 0}{R_E} = 0$$

Because of the controlled source, we need to write an “auxiliary” equation relating the control current (Δi_B) to node voltages:

$$\Delta i_B = \frac{v_i - v_o}{r_\pi}$$

Substituting the expression for Δi_B in our node equation, multiplying both sides by r_π , and collecting terms, we get:

$$v_i(1 + \beta) = v_o \left[1 + \beta + r_\pi \left(\frac{1}{r_o} + \frac{1}{R_E} \right) \right] = v_o \left[1 + \beta + \frac{r_\pi}{r_o \parallel R_E} \right]$$

Amplifier Gain can now be directly calculated:

$$A_v \equiv \frac{v_o}{v_i} = \frac{1}{1 + \frac{r_\pi}{(1 + \beta)(r_o \parallel R_E)}}$$

Unless R_E is very small (tens of Ω), the fraction in the denominator is quite small compared to 1 and $A_v \approx 1$.

To find the input impedance, we calculate i_i by KCL:

$$i_i = i_1 + \Delta i_B = \frac{v_i}{R_B} + \frac{v_i - v_o}{r_\pi}$$

Since $v_o \approx v_i$, we have $i_i = v_i/R_B$ or

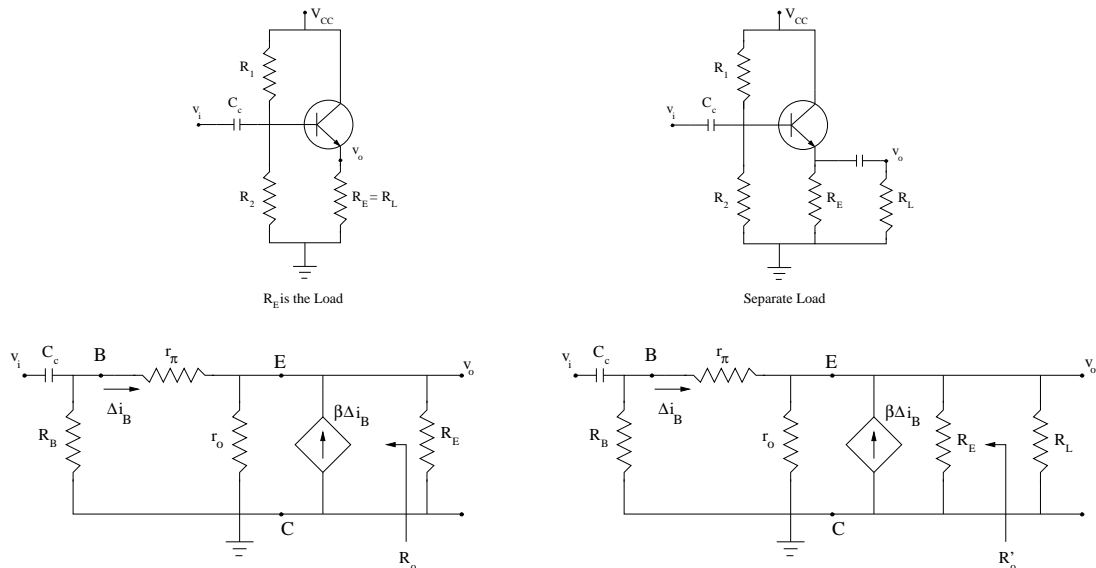
$$R_i \equiv \frac{v_i}{i_i} = R_B$$

Note that R_B is the combination of our biasing resistors R_1 and R_2 . With alternative biasing schemes which do not require R_1 and R_2 , (and, therefore $R_B \rightarrow \infty$), the input resistance of the emitter follower circuit will become large. In this case, we cannot use $v_o \approx v_i$. Using the full expression for v_o from above, the input resistance of the emitter follower circuit becomes:

$$R_i \equiv \frac{v_i}{i_i} = R_B \parallel [r_\pi + (R_E \parallel r_o)(1 + \beta)]$$

and it is quite large (hundreds of $k\Omega$ to several $M\Omega$) for $R_B \rightarrow \infty$. Such a circuit is in fact the first stage of the 741 OpAmp.

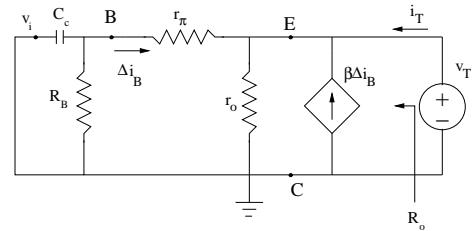
The output resistance of the common collector amplifier (in fact for all transistor amplifiers) is somewhat complicated because the load can be configured in two ways (see figure): First, R_E , itself, is the load. This is the case when the common collector is used as a “current amplifier” to raise the power level and to drive the load. The output resistance of the circuit is R_o as is shown in the circuit model. This is usually the case when values of R_o and A_i (current gain) is quoted in electronic text books.



Alternatively, the load can be placed in parallel to R_E . This is done when the common collector amplifier is used as a buffer ($A_v \approx 1$, R_i large). In this case, the output resistance is denoted by R'_o (see figure). For this circuit, BJT sees a resistance of $R_E \parallel R_L$. Obviously, if we want the load not to affect the emitter follower circuit, we should use R_L to be much

larger than R_E . In this case, little current flows in R_L which is fine because we are using this configuration as a buffer and not to amplify the current and power. As such, value of R'_o or A_i does not have much use.

When R_E is the load, the output resistance can be found by killing the source (short v_i) and finding the Thevenin resistance of the two-terminal network (using a test voltage source).



$$\text{KCL: } i_T = -\Delta i_B + \frac{v_T}{r_o} - \beta \Delta i_B$$

$$\text{KVL (outside loop): } -r_\pi \Delta i_B = v_T$$

Substituting for Δi_B from the 2nd equation in the first and rearranging terms we get:

$$R_o \equiv \frac{v_T}{i_T} = \frac{(r_o) r_\pi}{(1 + \beta)(r_o) + r_\pi} \approx \frac{(r_o) r_\pi}{(1 + \beta)(r_o)} = \frac{r_\pi}{(1 + \beta)} \approx \frac{r_\pi}{\beta} = r_e$$

where we have used the fact that $(1 + \beta)(r_o) \gg r_\pi$.

When R_E is the load, the current gain in this amplifier can be calculated by noting $i_o = v_o/R_E$ and $i_i \approx v_i/R_B$ as found above:

$$A_i \equiv \frac{i_o}{i_i} = \frac{R_B}{R_E}$$

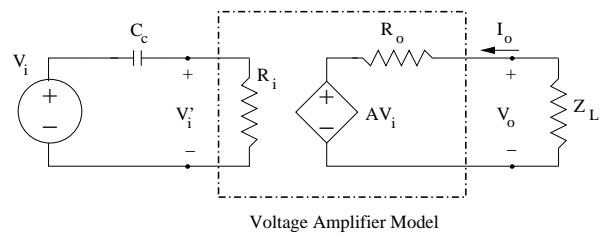
In summary, the general properties of the common collector amplifier (emitter follower) include a voltage gain of unity ($A_v \approx 1$), a very large input resistance $R_i \approx R_B$ (and can be made much larger with alternate biasing schemes). This circuit can be used as buffer for matching impedance, at the first stage of an amplifier to provide very large input resistance (such in 741 OpAmp). As a buffer, we need to ensure that $R_L \gg R_E$. The common collector amplifier can be also used as the last stage of some amplifier system to amplify the current (and thus, power) and drive a load. In this case, R_E is the load, R_o is small: $R_o = r_e$ and current gain can be substantial: $A_i = R_B/R_E$.

Impact of Coupling Capacitor:

Up to now, we have neglected the impact of the coupling capacitor in the circuit (assumed it was a short circuit). This is not a correct assumption at low frequencies. The coupling capacitor results in a lower cut-off frequency for the transistor amplifiers. In order to find the cut-off frequency, we need to repeat the above analysis and include the coupling capacitor

impedance in the calculation. In most cases, however, the impact of the coupling capacitor and the lower cut-off frequency can be deduced by examining the amplifier circuit model.

Consider our general model for any amplifier circuit. If we assume that the coupling capacitor is short circuit (similar to our AC analysis of BJT amplifier), $v'_i = v_i$.



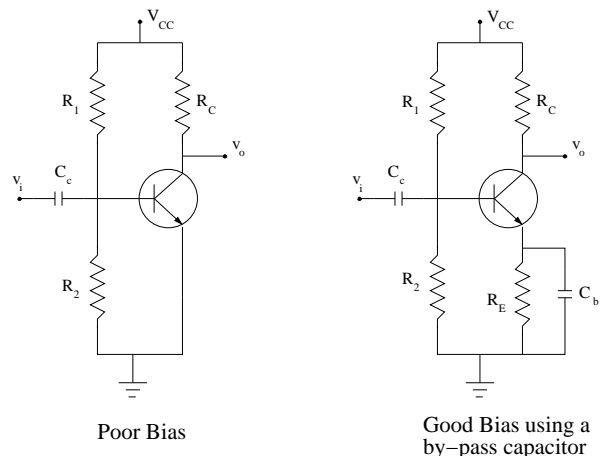
When we account for impedance of the capacitor, we have set up a high pass filter in the input part of the circuit (combination of the coupling capacitor and the input resistance of the amplifier). This combination introduces a lower cut-off frequency for our amplifier which is the same as the cut-off frequency of the high-pass filter:

$$\omega_l = 2\pi f_l = \frac{1}{R_i C_c}$$

Lastly, our small signal model is a low-frequency model. As such, our analysis indicates that the amplifier has no upper cut-off frequency (which is not true). At high frequencies, the capacitance between BE, BC, CE layers become important and a high-frequency small-signal model for BJT should be used for analysis. You will see these models in upper division courses. Basically, these capacitances result in amplifier gain to drop at high frequencies. PSpice includes a high-frequency model for BJT, so your simulation should show the upper cut-off frequency for BJT amplifiers.

Common Emitter Amplifier

DC analysis: Recall that an emitter resistor is necessary to provide stability of the bias point. As such, the circuit configuration as is shown has as a poor bias. We need to include R_E for good biasing (DC signals) and eliminate it for AC signals. The solution to include an emitter resistance and use a “bypass” capacitor to short it out for AC signals as is shown.



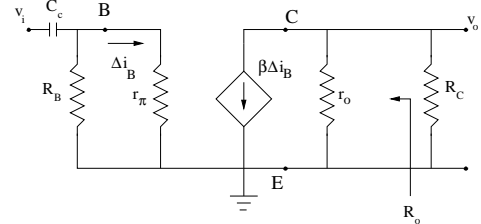
For this new circuit and with the capacitors open circuit, this circuit is the same as our good biasing circuit of page 78. The bias point currents and voltages can be found using procedure of pages 78-81.

AC analysis: To start the analysis, we kill all DC sources, combine R_1 and R_2 into R_B and replace the BJT with its small signal model. We see that emitter is now common between input and output AC signals (thus, common emitter amplifier. Analysis of this circuit is straightforward. Examination of the circuit shows that:

$$v_i = r_\pi \Delta i_B \quad v_o = -(R_c \parallel r_o) \beta \Delta i_B$$

$$A_v \equiv \frac{v_o}{v_i} = -\frac{\beta}{r_\pi} (R_c \parallel r_o) \approx -\frac{\beta}{r_\pi} R_c = -\frac{R_c}{r_e}$$

$$R_i = R_B \parallel r_\pi \quad R_o = r_o$$



The negative sign in A_v indicates 180° phase shift between input and output. The circuit has a large voltage gain but has medium value for input resistance.

As with the emitter follower circuit, the load can be configured in two ways: 1) R_c is the load. Then $R_o = r_o$ and the circuit has a reasonable current gain. 2) Load is placed in parallel to R_c . In this case, we need to ensure that $R_L \gg R_c$. Little current will flow in R_L and R_o and A_i values are of not much use.

Lower cut-off frequency: Both the coupling and bypass capacitors contribute to setting the lower cut-off frequency for this amplifier, both act as a low-pass filter with:

$$\omega_l(\text{coupling}) = 2\pi f_l = \frac{1}{R_i C_c}$$

$$\omega_l(\text{bypass}) = 2\pi f_l = \frac{1}{R'_E C_b}$$

where $R'_E \equiv R_E \parallel (r_e + \frac{R_B}{\beta})$

In the case when these two frequencies are far apart, the cut-off frequency of the amplifier is set by the “larger” cut-off frequency. *i.e.*,

$$\omega_l(\text{bypass}) \ll \omega_l(\text{coupling}) \quad \rightarrow \quad \omega_l = 2\pi f_l = \frac{1}{R_i C_c}$$

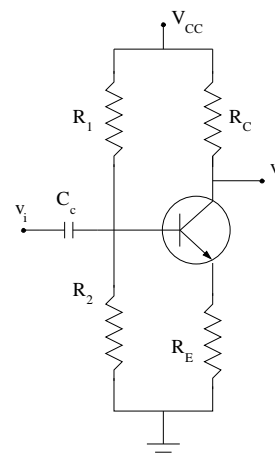
$$\omega_l(\text{coupling}) \ll \omega_l(\text{bypass}) \quad \rightarrow \quad \omega_l = 2\pi f_l = \frac{1}{R'_E C_b}$$

When the two frequencies are close to each other, there is no exact analytical formulas, the cut-off frequency should be found from simulations. An approximate formula for the cut-off frequency (accurate within a factor of two and exact at the limits) is:

$$\omega_l = 2\pi f_l = \frac{1}{R_i C_c} + \frac{1}{R'_E C_b}$$

Common Emitter Amplifier with Emitter resistance

A problem with the common emitter amplifier is that its gain depend on BJT parameters $A_v \approx (\beta/r_\pi)R_C$. Some form of feedback is necessary to ensure stable gain for this amplifier. One way to achieve this is to add an emitter resistance. Recall impact of negative feedback on OpAmp circuits: we traded gain for stability of the output. Same principles apply here.



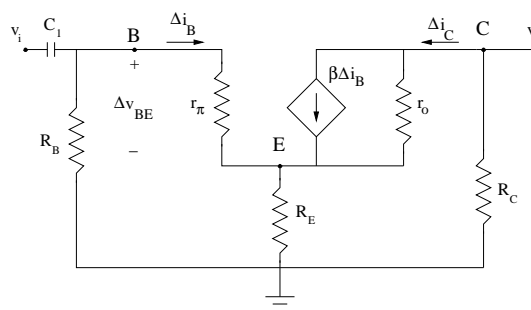
DC analysis: With the capacitors open circuit, this circuit is the same as our good biasing circuit of page 78. The bias point currents and voltages can be found using procedure of pages 78-81.

AC analysis: To start the analysis, we kill all DC sources, combine R_1 and R_2 into R_B and replace the BJT with its small signal model. Analysis is straight forward using node-voltage method.

$$\frac{v_E - v_i}{r_\pi} + \frac{v_E}{R_E} - \beta \Delta i_B + \frac{v_E - v_o}{r_o} = 0$$

$$\frac{v_o}{R_C} + \frac{v_o - v_E}{r_o} + \beta \Delta i_B = 0$$

$$\Delta i_B = \frac{v_i - v_E}{r_\pi} \quad (\text{Controlled source aux. Eq.})$$



Substituting for Δi_B in the node equations and noting $1 + \beta \approx \beta$, we get:

$$\frac{v_E}{R_E} + \beta \frac{v_E - v_i}{r_\pi} + \frac{v_E - v_o}{r_o} = 0$$

$$\frac{v_o}{R_C} + \frac{v_o - v_E}{r_o} - \beta \frac{v_E - v_i}{r_\pi} = 0$$

Above are two equations in two unknowns (v_E and v_o). Adding the two equation together we get $v_E = -(R_E/R_C)v_o$ and substituting that in either equations we can find v_o .

Alternatively, we can find compact and simple solutions by noting that terms containing r_o in the denominator are usually small as r_o is quite large. In this case, the node equations simplify to (using $r_\pi/\beta = r_e$):

$$v_E \left(\frac{1}{R_E} + \frac{1}{r_e} \right) = \frac{v_i}{r_e} \quad \rightarrow \quad v_E = \frac{R_E}{R_E + r_e} v_i$$

$$v_o = \frac{R_C}{r_e} (v_E - v_i) = \frac{R_C}{r_e} \left(\frac{R_E}{R_E + r_e} - 1 \right) v_i = -\frac{R_C}{R_E + r_e} v_i$$

Then, the voltage gain and input and output resistance can also be easily calculated:

$$A_v = \frac{v_o}{v_i} = -\frac{R_C}{R_E + r_e} \approx -\frac{R_C}{R_E}$$

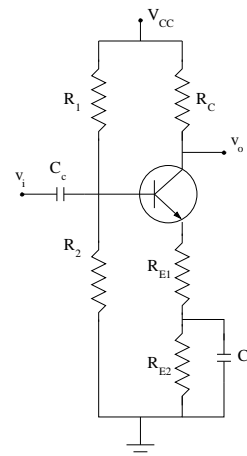
$$R_i = R_B \parallel [\beta(R_E + r_e)] \quad R_o = r_e$$

As before the minus sign in A_v indicates a 180° phase shift between input and output signals. Note the impact of negative feedback introduced by the emitter resistance. The voltage gain is independent of BJT parameters and is set by R_C and R_E as $R_E \gg r_e$ (recall OpAmp inverting amplifier!). The input resistance is increased dramatically.

Lower cut-off frequency: The coupling capacitor together with the input resistance of the amplifier lead to a lower cut-off frequency for this amplifier (similar to emitter follower). The lower cut-off frequency is given by:

$$\omega_l = 2\pi f_l = \frac{1}{R_i C_c}$$

A Possible Biasing Problem: The gain of the common emitter amplifier with the emitter resistance is approximately R_C/R_E . For cases when a high gain (gains larger than 5-10) is needed, R_E may become so small that the necessary good biasing condition, $V_E = R_E I_E > 1$ V cannot be fulfilled. The solution is to use a by-pass capacitor as is shown. The AC signal sees an emitter resistance of R_{E1} while for DC signal the emitter resistance is the larger value of $R_E = R_{E1} + R_{E2}$. Obviously formulas for common emitter amplifier with emitter resistance can be applied here by replacing R_E with R_{E1} as in deriving the amplifier gain, and input and output impedances, we “short” the bypass capacitor so R_{E2} is effectively removed from the circuit.



The addition of by-pass capacitor, however, modify the lower cut-off frequency of the circuit. Similar to a regular common emitter amplifier with no emitter resistance, both the coupling and bypass capacitors contribute to setting the lower cut-off frequency for this amplifier. Similarly we find that an approximate formula for the cut-off frequency (accurate within a factor of two and exact at the limits) is:

$$\omega_l = 2\pi f_l = \frac{1}{R_i C_c} + \frac{1}{R'_E C_b}$$

where $R'_E \equiv R_{E2} \parallel (R_{E1} + r_e + \frac{R_B}{\beta})$

Summary of BJT Amplifiers

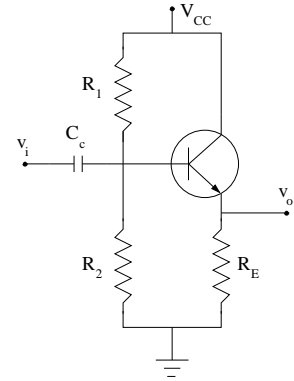
Common Collector (Emitter Follower):

$$A_v = \frac{(R_E \parallel r_o)(1 + \beta)}{r_\pi + (R_E \parallel r_o)(1 + \beta)} \approx 1$$

$$R_i = R_B \parallel [r_\pi + (R_E \parallel r_o)(1 + \beta)] \approx R_B$$

$$R_o = \frac{(r_o)r_\pi}{(1 + \beta)(r_o) + r_\pi} \approx \frac{r_\pi}{\beta} = r_e$$

$$2\pi f_l = \frac{1}{R_i C_c}$$



Common Emitter:

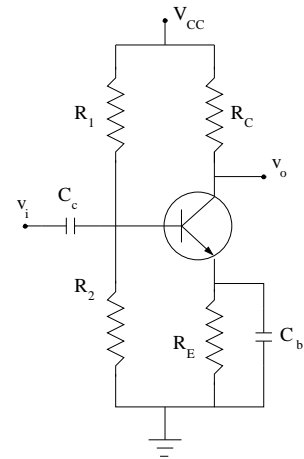
$$A_v = -\frac{\beta}{r_\pi}(R_c \parallel r_o) \approx -\frac{\beta}{r_\pi}R_c = -\frac{R_c}{r_e}$$

$$R_i = R_B \parallel r_\pi$$

$$R_o = r_o$$

$$2\pi f_l = \frac{1}{R_i C_c} + \frac{1}{R'_E C_b}$$

where $R'_E \equiv R_E \parallel (r_e + \frac{R_B}{\beta})$



Common Emitter with Emitter Resistance:

$$A_v = -\frac{R_C}{R_{E1} + r_e} \approx -\frac{R_C}{R_{E1}}$$

$$R_i = R_B \parallel [\beta(R_{E1} + r_e)]$$

$$R_o = r_e$$

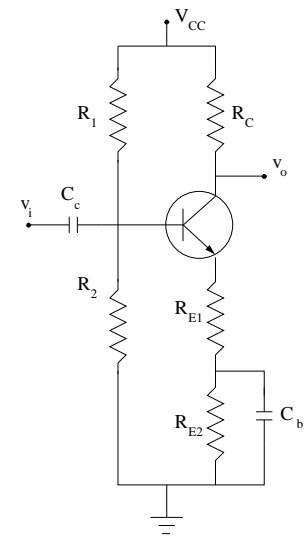
If R_{E2} and bypass capacitors are not present, replace R_{E1} with R_E in above formula and

$$2\pi f_l = \frac{1}{R_i C_c}$$

If R_{E2} and bypass capacitor are present,

$$\omega_l = 2\pi f_l = \frac{1}{R_i C_c} + \frac{1}{R'_E C_b}$$

where $R'_E \equiv R_{E2} \parallel (R_{E1} + r_e + \frac{R_B}{\beta})$



Examples of Analysis and Design of BJT Amplifiers

Example 1: Find the bias point and AC amplifier parameters of this circuit (Manufacturers' spec sheets give: $h_{fe} = 200$, $h_{ie} = 5 \text{ k}\Omega$, $h_{oe} = 10 \text{ }\mu\text{S}$).

$$r_{\pi} = h_{ie} = 5 \text{ k}\Omega \quad r_o = \frac{1}{h_{oe}} = 100 \text{ k}\Omega \quad \beta = h_{fe} = 200 \quad r_e = \frac{r_{\pi}}{\beta} = 25 \text{ }\Omega$$

DC analysis:

Replace R_1 and R_2 with their Thevenin equivalent and proceed with DC analysis (all DC current and voltages are denoted by capital letters):

$$R_B = 18 \text{ k} \parallel 22 \text{ k} = 9.9 \text{ k}\Omega$$

$$V_{BB} = \frac{22}{18 + 22} 9 = 4.95 \text{ V}$$

$$\text{KVL: } V_{BB} = R_B I_B + V_{BE} + 10^3 I_E \quad I_B = \frac{I_E}{1 + \beta} = \frac{I_E}{201}$$

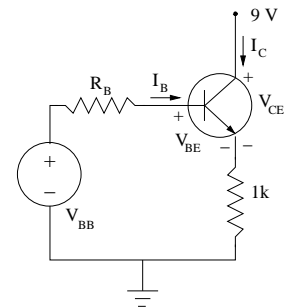
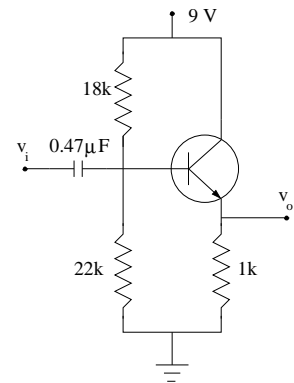
$$4.95 - 0.7 = I_E \left(\frac{9.9 \times 10^3}{2.1} + 10^3 \right)$$

$$I_E = 4 \text{ mA} \approx I_C, \quad I_B = \frac{I_C}{\beta} = 20 \text{ }\mu\text{A}$$

$$\text{KVL: } V_{CC} = V_{CE} + 10^3 I_E$$

$$V_{CE} = 9 - 10^3 \times 4 \times 10^{-3} = 5 \text{ V}$$

$$\text{DC Bias summary: } I_E \approx I_C = 4 \text{ mA}, \quad I_B = 20 \text{ }\mu\text{A}, \quad V_{CE} = 5 \text{ V}$$



AC analysis: The circuit is a common collector amplifier. Using the formulas in page 98,

$$A_v \approx 1$$

$$R_i \approx R_B = 9.9 \text{ k}\Omega$$

$$R_o \approx r_e = 25 \text{ }\Omega$$

$$f_l = \frac{\omega_l}{2\pi} = \frac{1}{2\pi R_B C_c} = \frac{1}{2\pi \times 9.9 \times 10^3 \times 0.47 \times 10^{-6}} = 36 \text{ Hz}$$

Example 2: Find the bias point and AC amplifier parameters of this circuit (Manufacturers' spec sheets give: $h_{fe} = 200$, $h_{ie} = 5 \text{ k}\Omega$, $h_{oe} = 10 \text{ }\mu\text{S}$).

$$r_{\pi} = h_{ie} = 5 \text{ k}\Omega \quad r_o = \frac{1}{h_{oe}} = 100 \text{ k}\Omega \quad \beta = h_{fe} = 200 \quad r_e = \frac{r_{\pi}}{\beta} = 25 \text{ }\Omega$$

DC analysis:

Replace R_1 and R_2 with their Thevenin equivalent and proceed with DC analysis (all DC current and voltages are denoted by capital letters). Since all capacitors are replaced with open circuit, the emitter resistance for DC analysis is $270 + 240 = 510 \text{ }\Omega$.

$$R_B = 5.9 \text{ k} \parallel 34 \text{ k} = 5.0 \text{ k}\Omega$$

$$V_{BB} = \frac{5.9}{5.9 + 34} 15 = 2.22 \text{ V}$$

$$\text{KVL: } V_{BB} = R_B I_B + V_{BE} + 510 I_E \quad I_B = \frac{I_E}{1 + \beta} = \frac{I_E}{201}$$

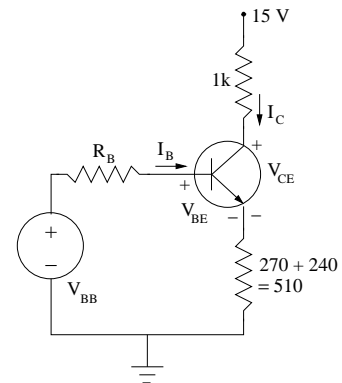
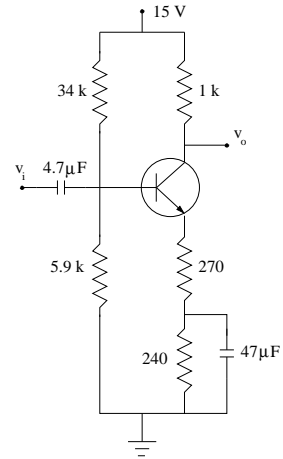
$$2.22 - 0.7 = I_E \left(\frac{5.0 \times 10^3}{2.1} + 510 \right)$$

$$I_E = 3 \text{ mA} \approx I_C, \quad I_B = \frac{I_C}{\beta} = 15 \text{ }\mu\text{A}$$

$$\text{KVL: } V_{CC} = 1000 I_C + V_{CE} + 510 I_E$$

$$V_{CE} = 15 - 1, 510 \times 3 \times 10^{-3} = 10.5 \text{ V}$$

$$\text{DC Bias: } I_E \approx I_C = 3 \text{ mA}, \quad I_B = 15 \text{ }\mu\text{A}, \quad V_{CE} = 10.5 \text{ V}$$



AC analysis: The circuit is a common collector amplifier with an emitter resistance. Note that the $240 \text{ }\Omega$ resistor is shorted out with the by-pass capacitor. It only enters the formula for the lower cut-off frequency. Using the formulas in page 98:

$$A_v = \frac{R_C}{R_{E1} + r_e} = \frac{1,000}{270 + 25} = 3.39$$

$$R_i \approx R_B = 5.0 \text{ k}\Omega \quad R_o \approx r_e = 25 \text{ }\Omega$$

$$R'_E \equiv R_{E2} \parallel (R_{E1} + r_e + \frac{R_B}{\beta}) = 240 \parallel (270 + 25 + \frac{5,000}{200}) = 137 \text{ }\Omega$$

$$f_l = \frac{\omega_l}{2\pi} = \frac{1}{2\pi R_i C_c} + \frac{1}{2\pi R'_E C_b} =$$

$$\frac{1}{2\pi \times 5,000 \times 4.7 \times 10^{-6}} + \frac{1}{2\pi \times 137 \times 47 \times 10^{-6}} = 31.5 \text{ Hz}$$

Example 3: Design a BJT amplifier with a gain of 4 and a lower cut-off frequency of 100 Hz. The Q point parameters should be $I_C = 3 \text{ mA}$ and $V_{CE} = 7.5 \text{ V}$. (Manufacturers' spec sheets give: $\beta_{min} = 100$, $\beta = 200$, $h_{ie} = 5 \text{ k}\Omega$, $h_{oe} = 10 \text{ }\mu\text{S}$).

$$r_\pi = h_{ie} = 5 \text{ k}\Omega \quad r_o = \frac{1}{h_{oe}} = 100 \text{ k}\Omega \quad r_e = \frac{r_\pi}{\beta} = 25 \text{ }\Omega$$

The prototype of this circuit is a common emitter amplifier with an emitter resistance. Using formulas of page 98 ($r_e = r_\pi/h_{fe} = 25 \text{ }\Omega$),

$$|A_v| = \frac{R_C}{R_E + r_e} \approx \frac{R_C}{R_E} = 4$$

The lower cut-off frequency will set the value of C_c .

We start with the DC bias: As V_{CC} is not given, we need to choose it. To set the Q-point in the middle of load line, set $V_{CC} = 2V_{CE} = 15 \text{ V}$. Then, noting $I_C \approx I_E$:

$$V_{CC} = R_C I_C + V_{CE} + R_E I_E$$

$$15 - 7.5 = 3 \times 10^{-3} (R_C + R_E) \quad \rightarrow \quad R_C + R_E = 2.5 \text{ k}\Omega$$

Values of R_C and R_E can be found from the above equation together with the AC gain of the amplifier, $A_V = 4$. Ignoring r_e compared to R_E (usually a good approximation), we get:

$$\frac{R_C}{R_E} = 4 \quad \rightarrow \quad 4R_E + R_E = 2.5 \text{ k}\Omega \quad \rightarrow \quad R_E = 500 \text{ }\Omega, R_C = 2. \text{ k}\Omega$$

Commercial values are $R_E = 510 \text{ }\Omega$ and $R_C = 2 \text{ k}\Omega$. Use these commercial values for the rest of analysis.

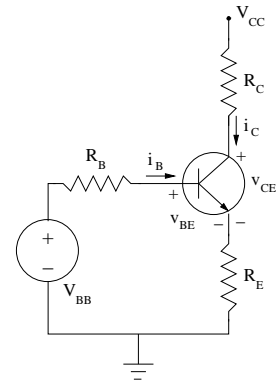
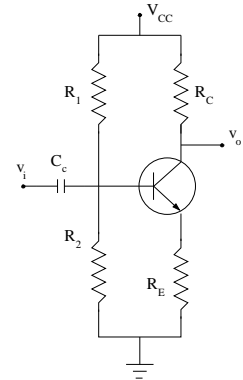
We need to check if $V_E > 1 \text{ V}$, the condition for good biasing. $V_E = R_E I_E = 510 \times 3 \times 10^{-3} = 1.5 > 1$, it is OK (See next example for the case when V_E is smaller than 1 V).

We now proceed to find R_B and V_{BB} . R_B is found from good bias condition and V_{BB} from a KVL in BE loop:

$$R_B \ll (\beta + 1)R_E \quad \rightarrow \quad R_B = 0.1(\beta_{min} + 1)R_E = 0.1 \times 101 \times 510 = 5.1 \text{ k}\Omega$$

$$\text{KVL: } V_{BB} = R_B I_B + V_{BE} + R_E I_E$$

$$V_{BB} = 5.1 \times 10^3 \frac{3 \times 10^{-3}}{201} + 0.7 + 510 \times 3 \times 10^{-3} = 2.28 \text{ V}$$



Bias resistors R_1 and R_2 are now found from R_B and V_{BB} :

$$R_B = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2} = 5 \text{ k}\Omega$$

$$\frac{V_{BB}}{V_{CC}} = \frac{R_2}{R_1 + R_2} = \frac{2.28}{15} = 0.152$$

R_1 can be found by dividing the two equations: $R_1 = 33 \text{ k}\Omega$. R_2 is found from the equation for V_{BB} to be $R_2 = 5.9 \text{ k}\Omega$. Commercial values are $R_1 = 33 \text{ k}\Omega$ and $R_2 = 6.2 \text{ k}\Omega$.

Lastly, we have to find the value of the coupling capacitor:

$$\omega_l = \frac{1}{R_i C_c} = 2\pi \times 100$$

Using $R_i \approx R_B = 5.1 \text{ k}\Omega$, we find $C_c = 3 \times 10^{-7} \text{ F}$ or a commercial values of $C_c = 300 \text{ nF}$.

So, are design values are: $R_1 = 33 \text{ k}\Omega$, $R_2 = 6.2 \text{ k}\Omega$, $R_E = 510 \Omega$, $R_C = 2 \text{ k}\Omega$. and $C_c = 300 \text{ nF}$.

Example 4: Design a BJT amplifier with a gain of 10 and a lower cut-off frequency of 100 Hz. The Q point parameters should be $I_C = 3 \text{ mA}$ and $V_{CE} = 7.5 \text{ V}$. A power supply of 15 V is available. Manufacturers' spec sheets give: $\beta_{min} = 100$, $h_{fe} = 200$, $r_\pi = 5 \text{ k}\Omega$, $h_{oe} = 10 \mu\text{S}$.

$$r_\pi = h_{ie} = 5 \text{ k}\Omega \quad r_o = \frac{1}{h_{oe}} = 100 \text{ k}\Omega \quad r_e = \frac{r_\pi}{\beta} = 25 \Omega$$

The prototype of this circuit is a common emitter amplifier with an emitter resistance. Using formulas of page 98:

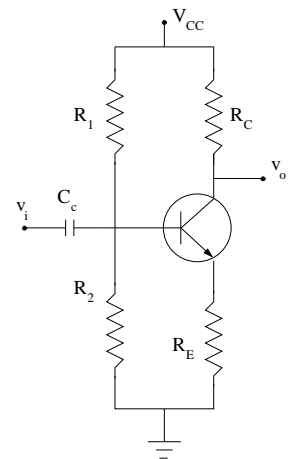
$$|A_v| = \frac{R_C}{R_E + r_e} \approx \frac{R_C}{R_E} = 10$$

The lower cut-off frequency will set the value of C_c .

We start with the DC bias: As the power supply voltage is given, we set $V_{CC} = 15 \text{ V}$. Then, noting $I_C \approx I_E$:

$$V_{CC} = R_C I_C + V_{CE} + R_E I_E$$

$$15 - 7.5 = 3 \times 10^{-3} (R_C + R_E) \quad \rightarrow \quad R_C + R_E = 2.5 \text{ k}\Omega$$



Values of R_C and R_E can be found from the above equation together with the AC gain of the amplifier $A_V = 10$. Ignoring r_e compared to R_E (usually a good approximation), we get:

$$\frac{R_C}{R_E} = 10 \quad \rightarrow \quad 10R_E + R_E = 2.5 \text{ k}\Omega \quad \rightarrow \quad R_E = 227 \text{ }\Omega, R_C = 2.27 \text{ k}\Omega$$

We need to check if $V_E > 1 \text{ V}$ which is the condition for good biasing: $V_E = R_E I_E = 227 \times 3 \times 10^{-3} = 0.69 < 1$. Therefore, we need to use a bypass capacitor and modify our circuits as is shown.

For DC analysis, the emitter resistance is $R_{E1} + R_{E2}$ while for AC analysis, the emitter resistance will be R_{E1} . Therefore:

$$\text{DC Bias:} \quad R_C + R_{E1} + R_{E2} = 2.5 \text{ k}\Omega$$

$$\text{AC gain:} \quad A_v = \frac{R_C}{R_{E1}} = 10$$

Above are two equations in three unknowns. A third equation is derived by setting $V_E = 1 \text{ V}$ to minimize the value of $R_{E1} + R_{E2}$.

$$V_E = (R_{E1} + R_{E2})I_E$$

$$R_{E1} + R_{E2} = \frac{1}{3 \times 10^{-3}} = 333$$

Now, solving for R_C , R_{E1} , and R_{E2} , we find $R_C = 2.2 \text{ k}\Omega$, $R_{E1} = 220 \text{ }\Omega$, and $R_{E2} = 110 \text{ }\Omega$ (All commercial values).

We can now proceed to find R_B and V_{BB} :

$$R_B \ll (\beta + 1)(R_{E1} + R_{E2})$$

$$R_B = 0.1(\beta_{min} + 1)(R_{E1} + R_{E2}) = 0.1 \times 101 \times 330 = 3.3 \text{ k}\Omega$$

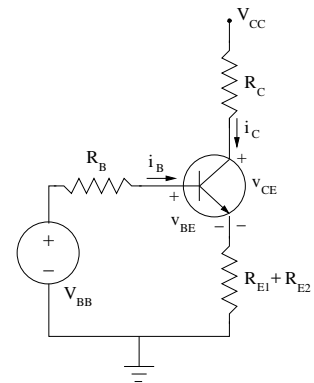
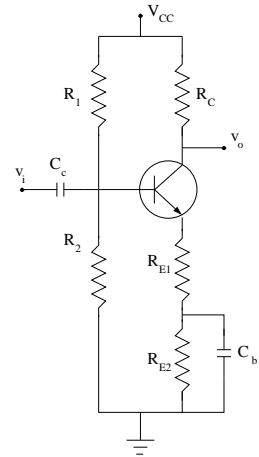
$$\text{KVL:} \quad V_{BB} = R_B I_B + V_{BE} + R_E I_E$$

$$V_{BB} = 3.3 \times 10^3 \frac{3 \times 10^{-3}}{201} + 0.7 + 330 \times 3 \times 10^{-3} = 1.7 \text{ V}$$

Bias resistors R_1 and R_2 are now found from R_B and V_{BB} :

$$R_B = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2} = 3.3 \text{ k}\Omega$$

$$\frac{V_{BB}}{V_{CC}} = \frac{R_2}{R_1 + R_2} = \frac{1}{15} = 0.066$$



R_1 can be found by dividing the two equations: $R_1 = 50 \text{ k}\Omega$ and R_2 is found from the equation for V_{BB} to be $R_2 = 3.6 \text{ k}\Omega$. Commercial values are $R_1 = 51 \text{ k}\Omega$ and $R_2 = 3.6 \text{ k}\Omega$

Lastly, we have to find the value of the coupling and bypass capacitors:

$$R'_E \equiv R_{E2} \parallel (R_{E1} + r_e + \frac{R_B}{\beta}) = 110 \parallel (220 + 25 + \frac{3,300}{200}) = 77.5 \Omega$$

$$R_i \approx R_B = 3.3 \text{ k}\Omega$$

$$\omega_l = \frac{1}{R_i C_c} + \frac{1}{R'_E C_b} = 2\pi \times 100$$

This is one equation in two unknown (C_c and C_b) so one can be chosen freely. Typically $C_b \gg C_c$ as $R_i \approx R_B \gg R_E \gg R'_E$. This means that unless we choose C_c to be very small, the cut-off frequency is set by the bypass capacitor. The usual approach is to choose C_b based on the cut-off frequency of the amplifier and choose C_c such that cut-off frequency of the $R_i C_c$ filter is at least a factor of ten lower than that of the bypass capacitor. Note that in this case, our formula for the cut-off frequency is quite accurate (see discussion in page 95) and is

$$\omega_l \approx \frac{1}{R'_E C_b} = 2\pi \times 100$$

This gives $C_b = 20 \mu\text{F}$. Then, setting

$$\frac{1}{R_i C_c} \ll \frac{1}{R'_E C_b}$$

$$\frac{1}{R_i C_c} = 0.1 \frac{1}{R'_E C_b}$$

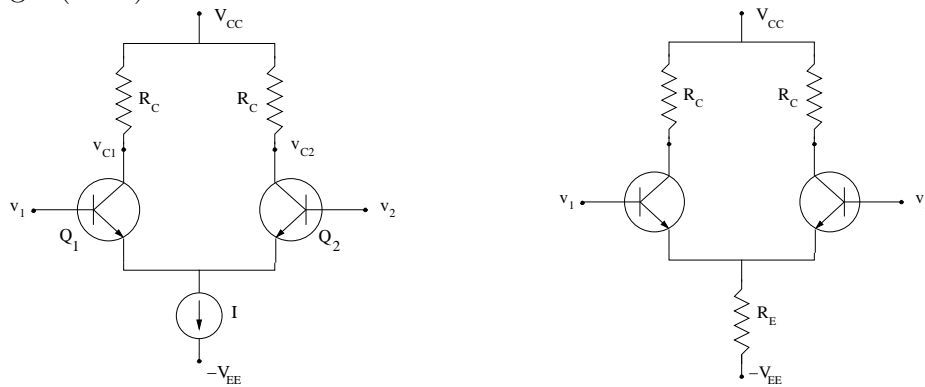
$$R_i C_c = 10 R'_E C_b \quad \rightarrow \quad C_c = 4.7^{-6} = 4.7 \mu\text{F}$$

So, are design values are: $R_1 = 50 \text{ k}\Omega$, $R_2 = 3.6 \text{ k}\Omega$, $R_{E1} = 220 \Omega$, $R_{E2} = 110 \Omega$, $R_C = 2.2 \text{ k}\Omega$, $C_b = 20 \mu\text{F}$, and $C_c = 4.7 \mu\text{F}$.

An alternative approach is to choose C_b (or C_c) and compute the value of the other from the formula for the cut-off frequency. For example, if we choose $C_b = 47 \mu\text{F}$, we find $C_c = 0.86 \mu\text{F}$.

BJT Differential Pairs: Emitter-Coupled Logic and Difference Amplifiers

The differential pairs are the most widely used circuit building block in analog ICs. They are made from both BJT and variant of Field-effect transistors (FET). In addition, BJT differential pairs are the basis for the very-high-speed logic circuit family called Emitter-Coupled Logic (ECL).



The circuit above (on the left) shows the basic BJT differential-pair configuration. It consists of two matched BJTs with emitters coupled together. On ICs, the differential pairs are typically biased by a current source as is shown (using a variant of current mirror circuit). The differential pair can be also biased by using an emitter resistor as is shown on the circuit above right. This variant is typically used when simple circuits are built from individual components (it is not very often utilized in modern circuits). Here we focus on the differential pairs that are biased with a current source.

The circuit has two inputs, v_1 and v_2 and the output signals can be extracted from the collector of both BJTs (v_{C1} and v_{C2}). Inspection of the circuit reveal certain properties. By KCL we find that $i_{C1} + i_{C2} \approx i_{E1} + i_{E2} = I$. That is the two BJTs share the current I between them. So, in general, $i_{C1} \approx i_{E1} \leq I$ and $i_{C2} \approx i_{E2} \leq I$. It is clear that at least one of the BJT pair should be ON (*i.e.*, not in cut-off) in order to satisfy the above equation (both i_{E1} and i_{E2} cannot be zero). Value of R_C is chosen such that either BJT will be in active-linear if its collector current reaches its maximum value of I .

$$V_{CC} = R_C i_{C1} + v_{CE1} + V_{ICS} - V_{EE}$$

$$v_{CE1} = V_{CC} + V_{EE} + V_{ICS} - R_C i_{C1} > v_\gamma$$

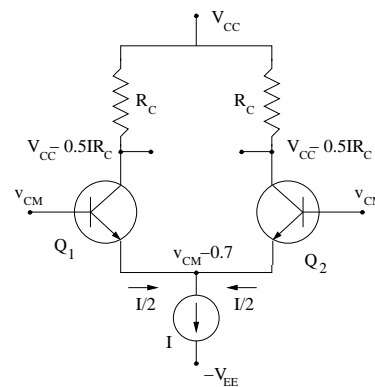
$$R_C < \frac{V_{CC} + V_{EE} + V_{ICS} - V_\gamma}{I} < \frac{V_{CC} + V_{EE} - V_\gamma}{I}$$

With this choice for R_C , both BJTs will either be in cut-off or active-linear (and never in saturation).

Lastly, if we write a KVL through a loop that contains the input voltage sources and both base-emitter junctions, we will have:

$$\text{KVL: } -v_1 + v_{BE1} - v_{BE2} + v_2 = 0 \quad \rightarrow \quad v_{BE1} - v_{BE2} = v_1 - v_2$$

To understand the behavior of the circuit, let's assume that a common voltage of v_{CM} is applied to both inputs: $v_1 = v_2 = v_{CM}$ (CM stands for Common Mode). Then, $v_{BE1} - v_{BE2} = v_1 - v_2 = 0$ or $v_{BE1} = v_{BE2}$. Because identical BJTs are biased with same v_{BE} , we should have $i_{E1} = i_{E2}$ and current I is divided equally between the pair:



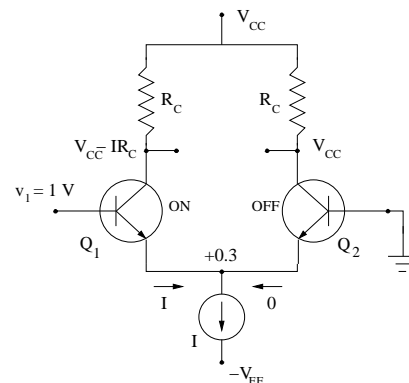
$$\text{KCL: } i_{C1} \approx i_{E1} = 0.5I \quad \text{and} \quad i_{C2} \approx i_{E2} = 0.5I.$$

As such, both BJTs will be in active linear, $v_{BE1} = v_{BE2} = 0.7$ V and the output voltages of $v_{C1} = v_{C2} = v_{CC} - 0.5IR_C$ will appear at both collectors.

Now, let's assume $v_1 = 1$ V and $v_2 = 0$. Writing KVL on a loop that contains both input voltage sources, we get:

$$\text{KVL: } v_{BE1} - v_{BE2} = v_1 - v_2 = 1 \text{ V}$$

Because $v_{BE} \leq v_\gamma = 0.7$ V, the only way that the above equation can be satisfied is for v_{BE2} to be negative: Q_2 is in cut-off and $i_{E2} = 0$. Because of the current sharing properties, Q_1 should be on and carry current I . Thus:



$$v_{BE1} = 0.7 \text{ V}, \quad v_{BE2} = v_{BE1} - 1 = -0.3 \text{ V}$$

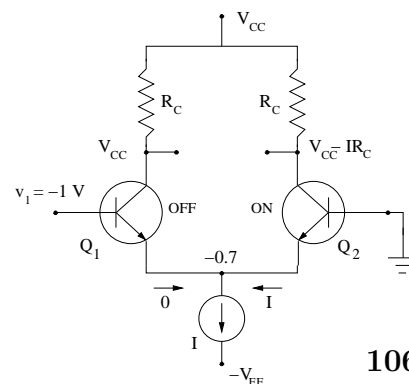
$$i_{C1} = i_{E1} = I, \quad i_{C2} = i_{E2} = 0$$

And voltages of $v_{C1} = V_{CC} - IR_C$ and $v_{C2} = V_{CC}$ will develop at the collectors of the BJT pair. One can easily show that for any $v_1 - v_2 > v_\gamma = 0.7$ V, Q_1 will be ON with $i_{C1} = i_{E1} = I$ and $v_{C1} = V_{CC} - IR_C$; and Q_2 will be OFF with $i_{C2} = i_{E2} = 0$ and $v_{C2} = V_{CC}$.

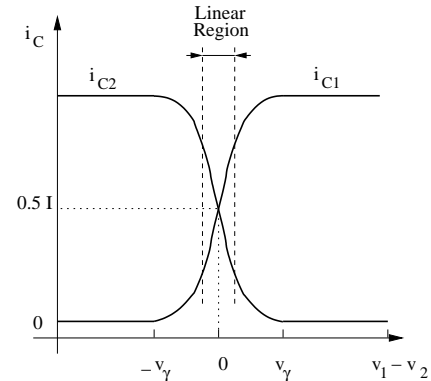
If we now apply $v_1 = -1$ V and $v_2 = 0$, the reverse of the above occurs:

$$\text{KVL: } v_{BE1} - v_{BE2} = v_1 - v_2 = -1 \text{ V}$$

In this case, Q_2 will be ON and carry current I and Q_1 will be OFF. Again, it is easy to show that this is true for any $v_1 - v_2 < -v_\gamma = -0.7$ V.



The response of the BJT differential pair to a pair of input signals with $v_d = v_1 - v_2$ is summarized in this graph. When v_d is large, the collector voltages switch from one state v_{CC} to another state $v_{CC} - IR_C$ depending on the sign v_d . As such, the differential pair can be used as a logic gate and a family of logic circuits, emitter-coupled logic, is based on differential pairs. In fact, because a BJT can switch very rapidly between cut-off and active-linear regimes, ECL circuits are the basis for very fast logic circuits today.



For small v_d (typically ≤ 0.2 V), the circuit behaves as a linear amplifier. In this case, the circuit is called a differential amplifier and is the most popular building block of analog ICs.

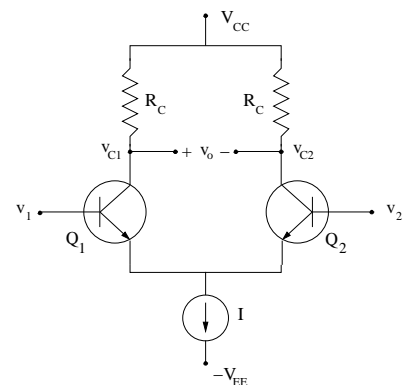
Differential Amplifiers

The properties of the differential amplifier above (case of v_d small) can be found in a straight-forward manner. The input signals v_1 and v_2 can be written in terms of their difference $v_d = v_1 - v_2$ and their average (common-mode voltage v_{CM}) as:

$$v_{CM} = \frac{v_1 + v_2}{2} \quad \text{and} \quad v_d = v_1 - v_2$$

$$v_1 = v_{CM} + 0.5v_d$$

$$v_2 = v_{CM} - 0.5v_d$$



The response of the circuit can now be found using superposition principle by considering the response to: case 1) $v_1 = v_{CM}$ and $v_2 = v_{CM}$ and case 2) $v_1 = 0.5v_d$ and $v_2 = -0.5v_d$. The response of the circuit to case 1, $v_1 = v_2 = v_{CM}$, was found in page 108. Effectively, v_{CM} sets the bias point for both BJTs with $i_{C1} = i_{E1} = i_{C2} = i_{E2} = 0.5I$, collector voltages of $v_{C1} = v_{C2} = v_{CC} - 0.5IR_C$, and a difference of zero between to collector voltages, $v_o = v_{C1} - v_{C2} = 0$.

To find the response of the circuit to case 2, $v_1 = 0.5v_d$ and $v_2 = -0.5v_d$, we can use our small signal model (since v_d is small). Examination of the circuit reveals that each of the BJTs form a common emitter amplifier configuration (with no emitter resistor). Using our analysis of common emitter amplifiers ($A_v = R_C/r_e$), we have:

$$v_{c1} = A_v v_i = \frac{R_C}{r_e} (0.5v_d) \quad \text{and} \quad v_{c2} = A_v v_i = \frac{R_C}{r_e} (-0.5v_d)$$

$$v_o = v_{c1} - v_{c2} = \frac{R_C}{r_e} v_d$$

Summing the responses for case 1 and 2, we find that the output voltage of this amplifier is

$$v_o = 0 + \frac{R_C}{r_e} v_d = \frac{R_C}{r_e} v_d \quad \rightarrow \quad A_v = \frac{R_C}{r_e}$$

similar to a common emitter amplifier. The additional complexity of this circuit compared to our standard common emitter amplifier results in three distinct improvements:

- 1) This is a “DC” amplifier and does not require a coupling capacitor.
- 2) Absence of biasing resistors ($R_b \rightarrow \infty$) leads to a higher input resistance, $R_i = r_\pi \parallel R_B = r_\pi$.
- 3) Elimination of biasing resistors makes it more suitable for IC implementation.

It should be obvious that a differential amplifier configuration can be developed which is similar to a common emitter amplifier with a emitter resistor (to stabilize the gain and increase the input resistance dramatically). Such a circuit is shown. Note that R_E in this circuit is not used to provide stable DC biasing (current source does that). Its function is to provide negative feedback for amplification of small signal, v_d . Following the above procedure, one can show that the gain of this amplifier configuration is:

$$v_o = \frac{R_C}{R_E + r_e} v_d \quad \rightarrow \quad A_v = \frac{R_C}{R_E + r_e}$$

As with standard CE amplifier with emitter resistance, the input impedance is also increased dramatically by negative feedback of R_E (and absence of biasing resistors, $R_b \rightarrow \infty$):

$$R_i = R_B \parallel [\beta(R_{E1} + r_e)] = \beta(R_{E1} + r_e)$$

