Exercise 1: Compute $i_D$ and $v_{DS}$ in the circuit below. MOS has $V_{t,n} = 0.4$ V and $\mu_n C_{ox} (W/L) = 1.0$ mA/V$^2$ for A) Ignoring channel-length modulation, b) Including channel-length modulation with $\lambda = 0.05$ V$^{-1}$.

- It is generally advantageous to solve for $V_{OV} = V_{GS} - V_t$ (instead of $V_{GS}$).

$$i_D = 0.5 \mu_n C_{ox} \frac{W}{L} V^2_{OV} \left[ 1 + \lambda v_{DS} \right]$$

- Ignoring channel length modulation introduces a relative error in circuit parameters (e.g., $i_D$) of $\sim \lambda v_{DS}$.
- This is an acceptable error in most biasing calculations.
\[ V_{OV} = v_{GS} - V_{t,n} = v_G - v_S - V_{t,n} = 1 - 0 - 0.4 = 0.6 \text{ V} \]

Assume Saturation*:\n\[ V_{OV} \geq 0 \text{ and } v_{DS} \geq V_{OV} \]

A) \( \lambda = 0 \)
Saturation: \[ i_D = 0.5 \mu_n C_{ox} \frac{W}{L} V_{OV}^2 = 0.5 \times 1.0 \times 10^{-3} \times (0.6)^2 = 0.180 \text{ mA} \]
KVL: \[ 1.8 = 5 \times 10^3 i_D + v_{DS} \Rightarrow v_{DS} = 1.8 - 5 \times 10^3 \times (0.18 \times 10^{-3}) = 0.90 \text{ V} \]
(\text{Expected error in } i_D \text{ and } v_{DS} \text{ is } \sim \lambda v_{DS} = 0.05 \times 0.90 = 4.5\%)

B) \( \lambda = 0.05 \text{ V}^{-1} \)
Saturation: \[ i_D = 0.5 \mu_n C_{ox} \frac{W}{L} V_{OV}^2 \left[ 1 + \lambda v_{DS} \right] = 0.18 \times 10^{-3} \left[ 1 + 0.05 v_{DS} \right] \]
KVL: \[ 1.8 = 5 \times 10^3 i_D + v_{DS} \Rightarrow 1.8 = 5 \times 10^3 \times (0.18 \times 10^{-3})(1 + 0.05 v_{DS}) + v_{DS} \]
\[ 1.8 = 0.9 + 0.045 v_{DS} + v_{DS} \Rightarrow v_{DS} = 0.86 \text{ V} \]
\[ i_D = 0.18 \times 10^{-3} \left[ 1 + 0.05 v_{DS} \right] = 0.188 \text{ mA} \]

*Note \( V_{OV} \geq 0 \text{ and } v_{DS} \geq V_{OV} \) for both cases, so assumption of saturation is justified.
Exercise 2: An NMOS $\mu_n C_{ox} (W/L) = 0.1 \text{mA/V}^2$ and $V_t = 0.5 \text{V}$ is to be operated in the saturation region. If $i_D = 12.5 \mu\text{A}$, find the required $v_{GS}$ and the minimum required $v_{DS}$. Ignore channel length modulation.

Saturation: $V_{OV} \geq 0$ and $v_{DS} \geq V_{OV}$

$i_D = 0.5\mu_n C_{ox} \frac{W}{L} \frac{V_{OV}^2}{V_{OV}} [1 + \lambda v_{DS}]$

$\lambda = 0 \implies i_D = 0.5\mu_n C_{ox} \frac{W}{L} V_{OV}^2$

$12.5 \times 10^{-6} = 0.5 (0.1 \times 10^{-3}) V_{OV}^2$

$V_{OV} = 0.5 \text{V}$

$v_{GS} = V_{OV} + V_t = 1 \text{V}$

For NMOS in saturation: $v_{DS} \geq V_{OV} = 0.5 \text{V} \implies$ Minimum $v_{DS} = 0.5 \text{V}$

An important aspect of amplifier design is to ensure that MOS is always in saturation.
Exercise 3: The PMOS transistor in the circuit below has $V_{t,p} = -0.5 \, \text{V}$. As the gate voltage, $v_G$, is varied from $+2.5 \, \text{V}$ to $0$, PMOS moves through all of its three states. Find values of $v_G$ at which the device changes modes of operation.

$v_{SD} = v_S - v_D = 2.5 - 1 = 1.5 \, \text{V}$

$V_{OV} = v_{SG} - |V_{t,p}| = v_S - v_G - |V_{t,p}| = 2.5 - v_G - 0.5 = 2.0 - v_G$

**Cut-Off:** $V_{OV} \leq 0 \Rightarrow 2.0 - v_G \leq 0 \Rightarrow v_G \geq 2.0 \, \text{V}$

**Triode:**

$V_{OV} \geq 0 \Rightarrow v_G \leq 2.0 \, \text{V}$

and

$v_{SD} \leq V_{OV} \Rightarrow 1.5 \leq V_{OV} = 2.0 - v_G \Rightarrow v_G \leq 2.0 - 1.5 = 0.5 \, \text{V}$

**Saturation:**

$V_{OV} \geq 0 \Rightarrow v_G \leq 2.0 \, \text{V}$

and

$v_{SD} \geq V_{OV} \Rightarrow 1.5 \geq V_{OV} = 2.0 - v_G \Rightarrow v_G \geq 2.0 - 1.5 = 0.5 \, \text{V}$

Transition from cut-off to saturation at $v_G = 2 \, \text{V}$

transition from saturation to triode at $v_G = 0.5 \, \text{V}$
Exercise 4: Find $V_S$ for $\mu_p C_{ox} (W/L) = 0.5 \text{ mA/V}^2$, $V_{tp} = -0.6 \text{ V}$ and $\lambda = 0$.

- Since $i_D = 40 \mu\text{A}$, PMOS is ON
- Assume PMOS in saturation

\[ i_D = 0.5 \mu_n C_{ox} \frac{W}{L} V_{OV}^2 \]
\[ 40 \times 10^{-6} = 0.5 \times 0.5 \times 10^{-3} V_{OV}^2 \rightarrow V_{OV} = 0.4 \text{V} \]

\[ v_{SG} = V_{OV} + |V_{tp}| = 0.4 + 0.6 = 1 \text{V} \]

\[ v_{SG} = V_S - V_G = V_S - 0 \rightarrow V_S = 1 \text{V} \]

\[ v_{SD} = V_S - V_D = 1 - (-5) = 6 \text{V} \]

\[ v_{SD} = 6 > V_{OV} = 0.4 \text{V} \] (PMOS in saturation)
Exercise 5: Find $V_1$ and $V_2$ ($\mu_n C_{ox} (W/L) = 5 \text{ mA/V}^2$, $V_t = 1 \text{ V}$, and ignore channel-length modulation).

GS1 - KVL: $0 = v_{GS1} + 10^3 i_D - 2.5 = V_{OV1} + V_t + 10^3 i_D - 2.5$

$\rightarrow V_{OV1} + 10^3 i_D = 1.5$

GS2 - KVL: $2.5 = v_{GS2} + v_{DS1} + 10^3 i_D - 2.5$

DS - KVL: $2.5 = v_{DS2} + v_{DS1} + 10^3 i_D - 2.5$

KCL: $i_{D1} = i_{D2} = i_D$

- Q1 is not in cut-off since for $i_{D1} = 0$, GS1-KVL gives $V_{OV} = 1.5 \text{ V} > 0$.
  - Q2 is not in cut-off either as $i_{D2} = i_D > 0$
Exercise 5 (cont’d): Find $V_1$ and $V_2$ ($\mu_n C_{ox} (W/L) = 5 \text{ mA/V}^2$, $V_t = 1 \text{ V}$, and ignore channel-length modulation).

Assume both MOS in saturation

\[
i_D = i_{D1} = 0.5 \mu_n C_{ox} \frac{W}{L} V_{OV1}^2
\]

GS1 - KVL:  
\[
1.5 = V_{OV1} + 10^3 i_D = V_{OV1} + 10^3 \times 0.5 \times 5 \times 10^{-3} V_{OV}^2
\]
\[
2.5 V_{OV1}^2 + V_{OV1} - 1.5 = 0
\]
\[
V_{OV1} = -1.0\text{V} \quad (\text{incorrect, need } V_{OV} > 0)
\]
\[
V_{OV1} = 0.60\text{V}
\]

Both MOS in saturation, $i_{D2} = i_{D1}$ and $\lambda = 0$: $V_{OV2} = V_{OV1} = 0.60 \text{ V}$

\[
v_{GS1} = V_{OV1} + V_t = 0.6 + 1 = 1.6 \text{ V}
\]
\[
v_{GS1} = V_{G1} - V_{S1} = 0 - V_2 \quad \to \quad V_2 = -1.6 \text{ V}
\]
\[
v_{GS2} = V_{OV2} + V_t = 0.6 + 1 = 1.6 \text{ V}
\]
\[
v_{GS2} = V_{G2} - V_{S2} = 2.5 - V_1 \quad \to \quad V_1 = 0.9 \text{ V}
\]
Exercise 5 (cont’d): Find $V_1$ and $V_2$ ($\mu_n C_{ox} (W/L) = 5 \text{ mA/V}^2$, $V_t = 1 \text{ V}$, and ignore channel-length modulation).

Need to confirm our assumption of both MOS in saturation

\[ \nu_{DS1} = V_{D1} - V_{S1} = V_1 - V_2 = 0.90 - (-1.6) = 2.5 \text{ V} \]
\[ \nu_{DS1} = 2.5 > V_{OV1} = 0.6 \text{ V} \]

\[ \nu_{DS2} = V_{D2} - V_{S2} = 2.5 - V_1 = 2.5 - 0.9 = 1.6 \text{ V} \]
\[ \nu_{DS2} = 1.6 > V_{OV2} = 0.6 \text{ V} \]

For circuits with multiple transistors, it is usually advantageous to keep track of node voltages (at transistor terminals!)