Note: You must do the circuit design, circuit analysis and PSpice simulations before coming to the Lab. For all experiments, OpAmps are powered with ±15 V supplies.

Part A – Schmitt Trigger:

Design: Design a Schmitt trigger with threshold voltages of −1 and +1 V. (Reading assignment: Section 10.5 of text book, pp 704-711)

PSpice Simulation: Set up the Schmitt trigger that you have designed. Apply a triangular wave with a frequency of 100 Hz and a peak-to-peak amplitude of 20 V (no DC offset) to the input. Simulate the circuit (transient analysis for several periods) and print out (on the same page) input and output waveforms. On the printout, mark the trigger voltage thresholds and compare them with your design values.

Lab Exercise:
1) Assemble the circuit on the breadboard (note commercial resistor values you are using in your actual circuit). Set the function generator to produce a triangular wave with a frequency of 100 Hz and a peak-to-peak amplitude of 20 V (no DC offset). Attach the function generator to the input and attache scopes channels A and B to input and output, respectively. Measure the trigger voltage thresholds and compare them with your design values. Print out the scope traces. Mark the trigger voltage thresholds on the printout. Compare your circuit performance with design values and PSpice simulations.

2) Set the scope into XY display mode (on display menu, set format to XY and persistence to 1 sec). Scope will display $v_o$ (as Y value) versus $v_i$ (as X value). This way, you should get the transfer characteristics of the Schmitt trigger. Make a printout of scope trace and label the axes and their scales.
Part B – Measurement of Diode iv Characteristics:

The circuit below allows one to measure the diode iv characteristics and find $I_s$ and $V_t$ by using a current-to-voltage converter circuit as is shown below.

Read Section 6.3 (pp 360-371) of the textbook. Note the diode equation:

$$i_D = I_s(e^{v_D/\eta V_t} - 1)$$

**Circuit Analysis:** Show that $v_i = v_D$ and $v_o = -i_D R_2$.

**Lab Exercise:** Set up the circuit on your breadboard. Apply a square wave at 1 kHz with no DC offset to the input. Use the 20dB attenuation output of the function generator and set the AC amplitude to zero before you connecting the function generator to the circuit. Display both $v_i$ and $v_o$ on the scope and center both signals so that zero voltage is in the middle of the scope of display. Slowly increase the amplitude of the input until the output square wave has an amplitude of about 10 V peak-to-peak. Because the input is a square wave, we are really applying only two distinct voltages to the input, call them high and low. For example, if the input has a peak-to-peak amplitude of 1 V, we are applying +0.5 (high) and −0.5 V (low) to the circuit. The output, therefore, will be a square wave, the high (low) voltage of output is proportional to diode current when the input is high (low). By measuring high and low voltages of $v_i$ and $v_o$, we will two iv pairs for the diode.

1) Explain why the output square wave is not symmetric around zero volt. (Hint: the high voltage of $v_o$ corresponds to diode being in the reverse bias and the low voltage of $v_o$ corresponds to diode being in the forward bias.)

2) Measure high and low voltages of $v_o$ and high and low voltages of $v_i$. Compute the two iv pair for the diode. Compute $I_s$.

3) Lower the input and repeat the experiment. Take about 8 measurements down to about 10 mV on $v_o$. (You may have to use the average (128) option under the Acquire menu to get a meaningful reading when $v_o$ becomes small.)

4) Tabulate your results, and make a linear and a semi-log plot of $i_D$ (Y axis) versus $v_D$. From the semi-log plot, estimate $V_t$ of the diode.
Part C – Diode Logic (DL) AND gate

Read pp 390-393 (Offset linear model of diode and DL AND Gate) of the text book. For analysis here, use the offset linear model given on top of the page 391 of the text book.

Circuit Analysis: 1) Consider the circuit below. $v_1$ and $v_2$ can be either 0 V (0 state) or 5 V (1 state). Compute $v_o$ for all possible combinations of $v_1$ and $v_2$. Make a table. From the voltage table, deduce the Truth table for this gate and show that it is an AND gate.

2) Compute $v_0$ when $v_1$ is floating (is not attached to anywhere) and $v_2 = 0$ and 5 V.

Lab exercise 1) Build the circuit. Use the power supply to set $v_1$ and $v_2$ either at 0 V (0 state) or 5 V (1 state). Note: in order to set $v_1$ or $v_2 = 0$, ground the terminal rather floating the terminal). Measure $v_o$ for all possible combinations of $v_1$ and $v_2$. Enter the experimental data in the table you have made in circuit analysis.

2) Measure $v_0$ when $v_1$ is floating and $v_2 = 0$ and 5 V. Compare to your calculations.