Note: Each student has to turn in this assignment.
Due Friday Jan. 17 in the class.
Attach the simulation circuit and all simulation results to your work.
Plots should be done by computer and/or by hand on graph paper.

Problem 1: Voltage Divider and PSPICE simulation of DC circuits

In many occasions we need to bias the circuit components with a voltage that is different than the power supply voltage. Other times we need to feed back a signal proportional to the output signal of one part of the circuit to another part. The voltage divider circuit below is the simplest circuit that does these functions and, therefore, is used extensively in the electronic circuits.

1) The voltage divider (the two resistors in the box) is a two-terminal network. Find the voltage transfer function and input and output impedances of this two-port network.

2) Plot the voltage transfer function of part 1 as a function of $R_L$. (Let $R_1 = 5 \, k\Omega$, $R_2 = 5 \, k\Omega$) for $R_L$ ranging from 0 to 50 $k\Omega$. On the graph, mark the value of voltage transfer function for $R_L \rightarrow \infty$. From the graph, show that voltage transfer function is maximum when $R_L \rightarrow \infty$. Also, show that the voltage transfer function is approximately independent of $R_L$ for $R_L \gg Z_o$.

3) Use PSpice to simulate the above circuit with $R_1 = 5 \, k\Omega$, $R_2 = 5 \, k\Omega$, $R_L = 5 \, k\Omega$, and $V_i = 10 \, V$. Use “Bias Point Details” option to find the value of $V_o$ and compare with results from part 1.
4) Assume $R_L$ is very large (i.e., open circuit). Use PSPICE to simulate the above circuit with $R_1 = 5 \, k\Omega$, $R_2 = 5 \, k\Omega$. Use DC SWEEP to generate a plot of $V_o$ as a function of $V_i$ for $V_i$ ranging from 0 to +10 V. Compare the simulation plot with the results from part 1.

5) Use PSPICE to simulate the above circuit with $R_1 = R_2 = 5 \, k\Omega$, and $V_i = 10 \, V$. Use parametric SWEEP to generate a plot of $V_o/V_i$ as a function of $R_L$ for $R_L$ ranging from 0 to 50 $k\Omega$ (choose the increment in $R_L$ such that you have a meaningful plot, i.e., the curve looks nice and smooth). Attach the plot to your work and compare the results with Part 2.

6) Use the simulation above and plot $I_o$ (current in $R_L$) versus $V_o$. This is the IV characteristics of the voltage divider circuit. Use this plot to find the output resistance of the voltage divider circuit. Compare with your analytical calculations of part 2.

7) **Design Problem:** Now let’s put what we have learned to practice. We have a transistor radio powered by a nine volt battery. We need to bias a transistor circuit in the radio with a voltage of approximately 4.5 V. Draw the voltage divider circuit that can do this, modeling the transistor circuit with a resistance (load). The maximum current drawn by this transistor is 0.45 mA (What is the minimum effective load resistance?). Find the best values of $R_1$ and $R_2$. Remember that we want to build this circuit so $R_1$ and $R_2$ should be available commercially.

You can use the following commercial resistor values: 1, 1.1, 1.2, 1.3, 1.5, 1.6, 1.8, 2, 2.2, 2.4, 2.7, 3., 3.3, 3.6, 3.9, 4.3, 4.7, 5.1, 5.6, 6.2, 6.8, 7.5, 8.2, 9.1 ($\times 10^n$ where $n$ is an integer)

**Problem 2:** An exercise with complex numbers and plotting.

Consider the function $H(jf) = \frac{10}{1 + j(f/f_0)}$ where $j = \sqrt{-1}$.

a) Derive analytical expressions for the amplitude and phase of $H$.

b) What is maximum value of amplitude of $H$. What is the minimum value of amplitude of $H$.

c) Plot a linear-linear plot of $|H|$ as a function of $f/f_0$ for $f/f_0$ ranging from 0.1 to 10.

d) Plot a log-log plot of $|H|$ as a function of $f/f_0$ for $f/f_0$ ranging from 0.1 to 10.

e) Plot a semi-log plot of phase of $H$ as a function of $f/f_0$ for $f/f_0$ ranging from 0.1 to 10. (Use linear axis for phase of $H$ and a log axis for $f$).